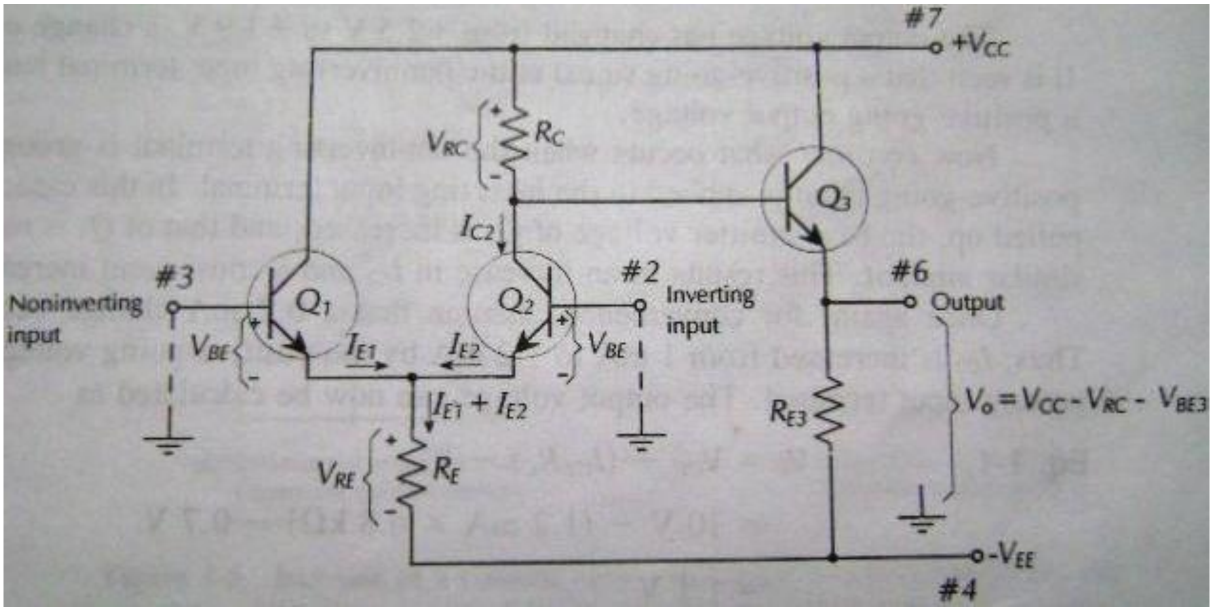
UNIT - 1

OPERATIONAL AMPLIFIER FUNDAMENTALS

1.1 Basic operational amplifier circuit-



The basic circuit of an operational amplifier is as shown in above fig. has a differential amplifier input stage and an emitter follower output. Supply voltages $+V_{cc}$ and $-V_{cc}$ are provided. Transistors Q_1 and Q_2 constitute a differential amplifier, which produces a voltage change as the collector of Q_2 where a difference input voltage is applied to the bases of Q_1 and Q_2. Transistor Q_2 operates as an emitter follower to provide low output impedance.

$$V_o = V_{cc} - V_{RC} - V_{BE3}$$

$$= V_{cc} - I_{C2}R_c - V_{BE}$$

Assume that Q_1 and Q_2 are matched transistors that are they have equal V_{BE} levels and equalcurrent gains.

With both transistor bases at ground level, the emitter currents are equal and both I_{E1} and I_{E2} flow through the common emitter resistor R_E.

The emitter current is given by:-

$$I_{E1} + I_{E2} = V_{RE}/R_E$$

With Q_1 and Q_2 bases grounded,

$$0 - V_{BE} - V_{RE} + V_{EE} = 0$$

$$V_{EE} - V_{BE} = V_{RE}$$

$$V_{RE} = V_{EE} - V_{BE}$$

$$I_{E1} + I_{E2} = \frac{V_{EE} - V_{BE}}{R_E}$$

$$V_{cc} = 10\text{ V},\ V_{EE} = -10\text{ V},\ R_E = 4.7\text{ K},\ R_c = 6.8\text{ K},\ V_{BE} = 0.7,$$

$$I_{E1} + I_{E2} = (10 - 0.7)/4.7\text{ K} + 2\text{ mA}$$

$$I_{E1} = I_{E2} = 1\text{mA}$$

$$I_{c2} = I_{E2} = 1\text{ mA}$$

$$V_o = 10 - 1\text{mA} \times 6.8\text{ K} - 0.7$$

$$V_o = 2.5\text{ V}$$

If a positive going voltage is applied to the non-inverting input terminal, Q_1 base is pulled up by the input voltage and its emitter terminal tends to follow the input signal. Since Q_1 and Q_2 emitters are connected together, the emitter of Q_2 is also pulled up by the positive going signal at the non-inverting input terminal. The base voltage of Q_2 is fixed at ground level, so the positive going movement at its emitter causes a reduction in its base-emitter voltage (V_{BE2}). The result of the reduction in V_{BE2} is that its emitter current is reduced and consequently its collector current is reduced.

Positive going input at the base of Q_1 reduces I_{c2} by 0.2 mA (from 1mA to 0.8mA)

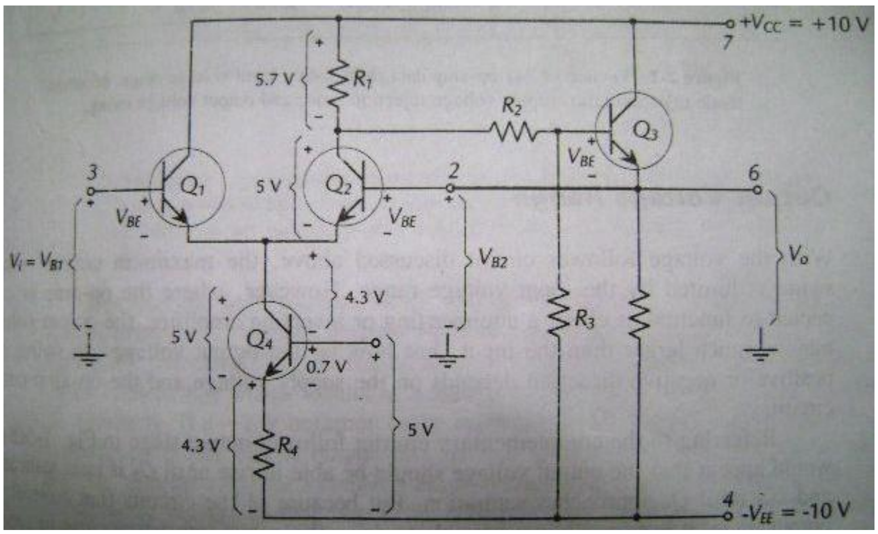
VO = 10 – (0.8 mA x 6.8 KΩ) – 0.7 = 3.9 V

It is seen that a positive going signal at pin 3 has produced a positive going output voltage

A basic operational amplifier circuit consists of a differential amplifier stage with two input terminals and a voltage follower output stage. The differential amplifier offers high impedance at both input terminals and it produces voltage gain. The output stage gives the op-amp low op output impedance. A practical op-amp circuit is much more complex than the basic circuit.

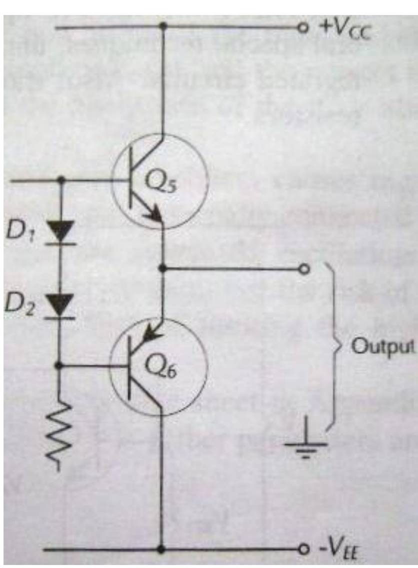
The circuit is designed to have a V_{CE} of 5V across Q2 and Q4. With a ±10 V supply and the bases of Q1 and Q2 at ground level, the voltage drops across R1 and R4 is 5.7 V and 4.3 V respectively. If the input voltage at Q1 base goes down to -4 V, the output terminal and Q2 base also goes down to -4 V as the output follows the input.

This means that the emitter terminals of Q1 and Q2 are pushed down from -0.7 to -4.7 V. Consequently, the collector of Q4 is pushed down by 4 V, reducing V_{CE4} from 5 V to 1 V. Although Q4 might still be operational with a V_{CE} of 1 V, it is close to saturation. It is seen that there is a limit to the negative going input voltage that can be applied to the op-amp if the circuit is to continue to function correctly.



There is also a limit to positive going input voltages. Where V_{B1} goes to +4 V, the voltage drop across resistor R1 must be reduced to something less than 1 V, in order to move V_{B2} and V_{E3} up by 4 V to follow the input. This requires a reduction in I_{c2} to a level that makes Q2 approach cutoff. heT input voltage cannot be allowed to become large enough to drive Q2 into cutoff.

The maximum positive going and negative going input voltage that may be applied to an op-amp is termed as its input range.



OUTPUT VOLTAGE RANGE

The maximum voltage swing is limited by the input voltage range. The output voltage can swing in a positive or negative direction depends on the supply voltage and the op-amp output circuitry. Referring to the complementary emitter follower output stage in fig., it would appear that the output voltage should be able to rise until Q5 is near saturation and fall until Q6 approaches saturation.

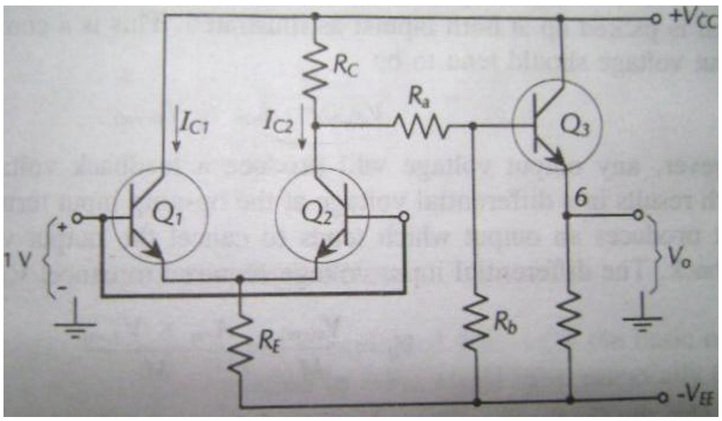
But because of the circuits that control the output stage, is normally not possible to drive the output transistors close to saturation levels.

A rough approximation for most op-amps is that the maximum output voltage swing is approximately equal to 1 V less than the supply voltage.

For the 741 op-amp with a supply of ±15 V, the data sheet lists the output voltage swing as typically ±14 V.

COMMON MODE AND SUPPLY REJECTION

Common mode rejection:-



When the same voltage is applied to both the input terminals of op-amp, the voltage is called 'Common Mode Voltage V_{in}', and the op-amp is said to be operating in the ' Common Mode Configuration '. Both input terminals are at the same potential, so ideally the output should be zero. Because the base voltages of Q_1 and Q_2 are biased to 1 V above ground, the voltage drop across emitter resistor R_E is increased by 1 V and consequently, I_{C1} and I_{C2} are increased. The increased level of I_{C2} produces an increased voltage drop across R_C , which results in a change in the output voltage at the emitter of Q_3.

The common mode gain is given by,

$$A_{cm} = \frac{V_{ocm}}{V_{icm}}$$

The success of the op-amp rejecting common mode inputs is defined in the common mode rejection ratio (CMRR). This is the ratio of the open loop gain A to the common mode gain A_{cm}.

$$CMRR = A/A_{cm}$$

It is expressed in decibel, CMRR = 20 log A/A_{cm}dB. The typical value of 741 is 90 dB.

Significance:

The CMRR expresses the ability of an op-amp to reject a common mode signal. Higher the value of CMRR, better is its ability to reject a common mode signal. Thus any unwanted signals such as noise or pickup would appear as common to both the input terminals and therefore the output due to this signal would be zero. Hence no undesirable noise signal will be amplified along with the desired signal.

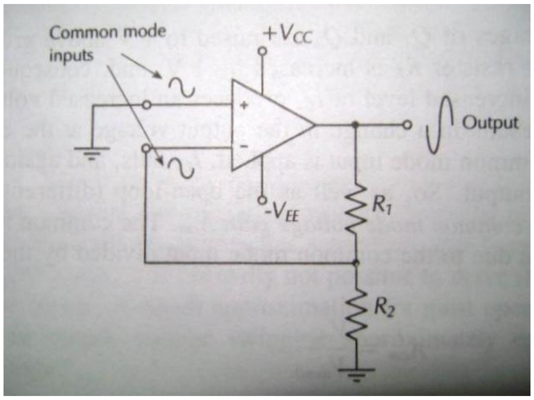
Consider the non-inverting amplifier circuit as shown below, with the input terminal grounded. The circuit output should also be at ground level. Now, suppose a sine wave signal is picked up at both inputs, this is a common mode input. The output voltage should tend to be,

$$V_{o\ cm} = A_{cm} \times V_{i\ cm}$$

Any output voltage will produce a feedback voltage across resistor R_i, which results in a differential voltage at the op-amp input terminals. The differential input produces an output which tends to cancel the output voltage that caused the feedback. The differential input voltage required to cancel $V_{o\ cm}$ is,

$$V_d = \frac{V_{o\ cm}}{A} = A_{cm} \times \frac{A_{cm} \times V_{i\ cm}}{A}$$

V_d is the feedback voltage developed across R_1



$$V_{dc} = \frac{R1}{R1+Rf} \times V_{ocm}$$

$$\frac{R1}{R1+Rf} \times V_{o(cm)} = \frac{A_{cm} \times V_{i\ cm}}{A}$$

$$V_{o(cm)} = \frac{A_{cm} \times V_{i\ cm}}{A} \times \frac{R1}{R1+Rf}$$

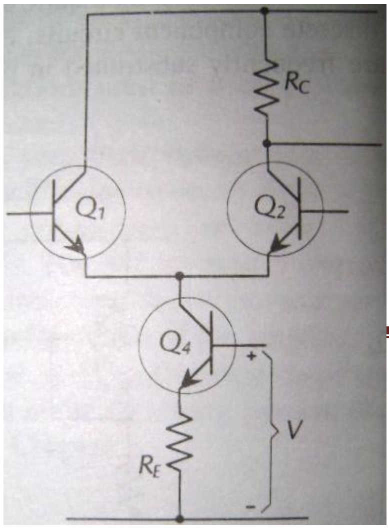
$$V_{o(cm)} = \frac{V_{i\ cm}}{CMRR} \times A_f$$

Problem

A 741 op-amp is used in a non-inverting amplifier with a voltage of 50. Calculate the typical output voltage that would result from a common mode input with a peak level of 100mV.

Solution

Typical value of CMRR for 741 op-amp = 90 dB.



$$CMRR = \text{antilog}\frac{90\ db}{20} = 31623$$

We have, $V_{ocm} = \frac{V_{i\ cm}}{CMRR} \times A_f$

$$= \frac{100\ mV}{CMRR} \times 50$$

Therefore, $V_{ocm} = 158\ \mu V$

POWER SUPPLY VOLTAGE REJECTION:

Any change in $-V_{EE}$ would produce a change in the voltage drop across R_E. This would result in an alteration in I_{E1}, I_{E2} and I_{C2}. The change in I_{C2} would alter V_{RC} and thus affect the level of the dc output voltage. The variation in $-V_{EE}$ would have an effect similar to an input voltage.

This can be minimized by replacing the emitter resistor with constant current circuit (or constant current tail) as shown in fig below.

A constant voltage drop is maintained across resistor R_E by providing a constant voltage V at Q_4 base. Now, any change in supply voltage is developed across the collector-emitter terminal of Q_4 and the emitter currents of Q_1 and Q_2 are not affected. Even with such circuitry, variations in V_{CC} and V_{EE} do produce some changes at the output. The Power Supply Rejection Ratio (PSRR) is a measure of how effective the op-amp is in dealing with variations in supply voltage.

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If a variation of 1V in V_{CC} or V_{EE} causes the output to change by 1V, then the supply voltage rejection ratio is 1V/V. If output changes by 10mV when one of the supply voltages hanges by 1V, then SVRR is 10mV/V. In 741 op-amps it is 30 mV/V.

<u>**Problem**</u>

A 741 op-amp uses a ± 15 V supply with 2 mV, 120 Hz ripple voltage superimposed. Calculate the amplitude of the output voltage produced by the power supply ripple.

$$V_o(rip) = Vs\ (rip) \times PSRR$$

$$= 2mV \times 30\mu V/V$$

$$= 60\ nV$$

OFFSET VOLTAGE AND CURRENTS:

Input offset voltage

Basic operational circuit connected to function as a voltage follower as shown in fig 2. The output terminal and the inverting terminal follow the voltage at the non-inverting input.

For the output voltage to be exactly equal to the input voltage, transistors Q1 and Q2 must be perfectly matched. The output voltage can b e calculated as,

$$V_o = V_i - V_{BE} + V_{BE2}$$

With $V_{BE1} = V_{BE} \rightarrow V_o = V_i$

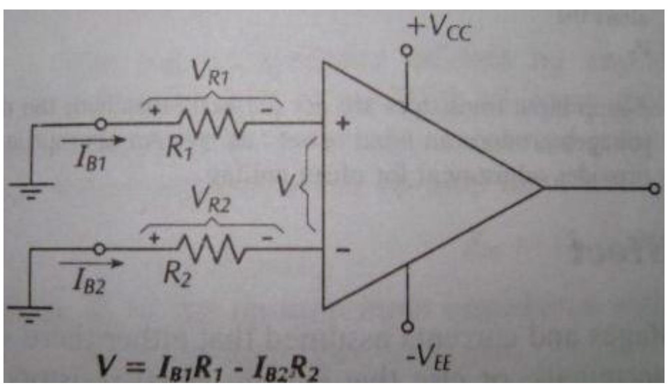
If the input voltage is zero then output voltage is also zero. i.e., $V_o = V_i$.

Suppose that the transistors are not perfectly matched and that V_{BE1} = 0,7 V while V_{BE2} = 0.6 V with the input at ground level,

$$V_o = 0 - 0.7V + 0.6V = - 0.1V$$

This unwanted output is known as 'Output Offset Voltage'. To set V_o to ground level the input would have to be raised to + 0.1V (i.e. the input voltage applied to reduce the output offset voltage to zero) is known as 'Input Offset Voltage'. Although transistors in integrated circuits are very well matched, there is always some input offset voltage. The typical offset voltage is listed as 1 mV on 741 data sheet (max –5 mV).

Input Offset Current



If the input transistors of an op-amp not being perfectly matched, as well as the transistor base-emitter voltages being unequal, the current gain of one transistor may not be exactly equal to that of the other. Thus, when both transistors have equal levels of collector current, the base current may not be equal. So, the algebraic difference between these input currents (base currents) is referred as 'Input Offset Current (I_{OS}) '.

$$I_{OS} = I\, I_{B1} - I_{B2}\, I$$

I_{B1} = Current in the non-inverting input

I_{B2} = Current in the inverting input

This typical value for 741 op-amps is 20 nA (min) and the max is 200 nA.

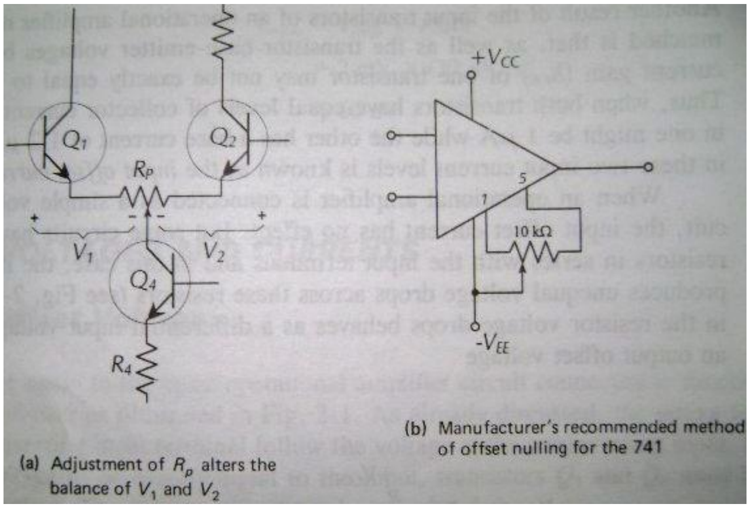
Input Bias Current (I_B)

Input bias current is the average of the currents that flow in to the inverting and non-inverting input terminals of the op-amp.

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

Typical value of input bias current I_B for 741 op-amps is 80 nA and max is 600 nA.

Offset Nulling



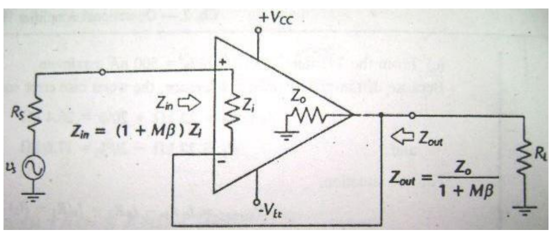
(a) Adjustment of R_p alters the balance of V_1 and V_2

(b) Manufacturer's recommended method of offset nulling for the 741

One method of dealing with input offset voltage and current is as shown in fig below, which shows a low resistance potentiometer (R_P) connected at the emitters of Q1 and Q2. Adjustment of RP alters the total voltage drop from each base to the common point at the potentiometer moving contact, because an offset voltage is produced by the input offset current. This adjustment can null the effects of both input offset current and input offset voltage.

INPUT AND OUTPUT IMPEDANCE

Input Impedance :



The input impedance offered by any op-amp is substantially modified by its application. From negative feedback theory, the impedance at the op-amp input terminal becomes,

$$Z_{ip} = (1 + A\beta)\, Z_i$$

Z_i = the op-amp input impedance without negative feedback.

A = op-amp open loop gain, typical value for 741 op-amp is 50000

β = Feed back factor

R_i= Input impedance, typical value for 741 op-amp is 0.3 MΩ

Output impedance:

The typical output resistance specified for the 741 op-amp is 75Ω. Any stray capacitance in parallel with this is certain to have a much larger resistance than 75Ω. So 75Ω is also effectively the amplifier output impedance.

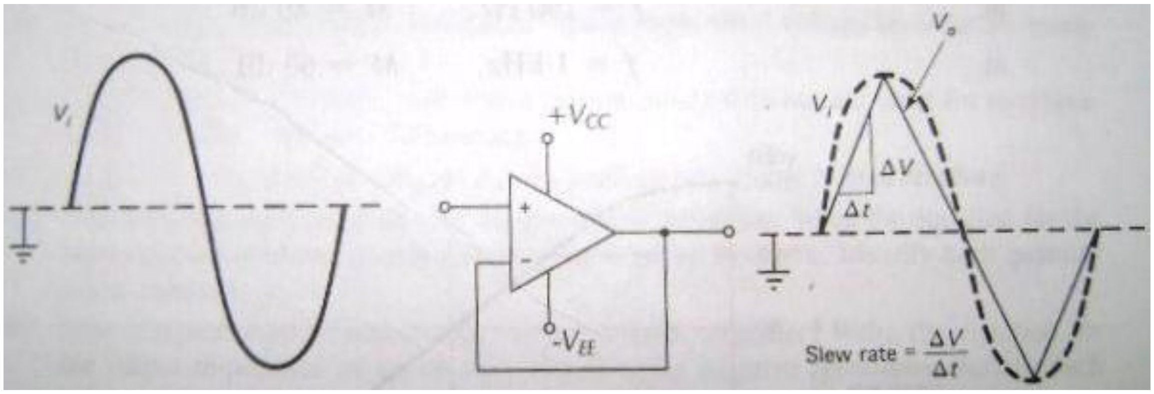
The output impedance of the op-amp is affected by ne gativfeedback.

$Z_{out} = \frac{Zo}{(1+A\beta)}$

Z_o = op-amp output impedance without negative feedback

Slew Rate

The slew rate (S) of any op-amp is the maximum rate at which the output voltage can change. When the slew rate is too slow for the input, distortion results. This is illustrated in fig below, which shows a sine wave input to a voltage follower producing a triangular output waveform. The triangular wave results because the op-amp output simply cannot fast enough to follow thee sine wave input.



$S = \frac{\Delta V_o}{t}$

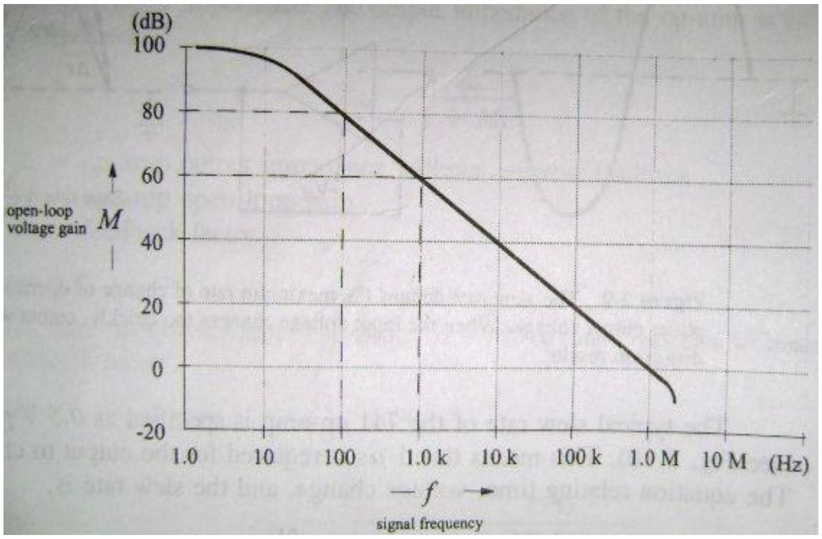
The typical slew rate of the 741 op-amp is 0.5 V/µs. This means that 1µs is required of output to change by 0.5 V

Frequency limitations

Fig below shows the graph of open loop gain (A) plotted versus frequency (f) for a 741 op-amp.

f = 100 Hz, A = 80 dB

f = 1 KHz, A = 60 dB



The open loop gain (A) falls by 20 dB when the frequency increases from 100 Hz to 1 KHz. The ten times increase in frequency is termed a decade. So, the rate of the gain is said to be 20 dB per decade. Where internal gain equals to or greater than 80 dB is required for a particular application, it is available with a 741 only for signal frequencies up to ≈100 Hz. A greater than 20 dB is possible for signal frequencies up to ≈ 90 kHz. Other op-amp maintains substantial internal gain to much higher frequencies than the 741.

1.2 OP-AMP AS DC AMPLIFIERS: Biasing op-amps

Bias Current Paths :

Op-amps must be correctly biased if they are to function properly. The inputs of most op-amps are the base terminals of the transistors in a differential amplifier. Base currents must flow into these terminals for the transistors to be operational.

One of the two input terminals is usually connected in some way to the op-amp output to facilitate negative feedback. The other input might be biased directly to ground via a signal source.

From the fig given below, current I_{B1} flows into the op-amp via the signal source while I_{B2} flows from the output terminal. The next fig shows a situation in which resistor R1 is added in series with inverting terminal to match signal source resistance Rs in series with the non-inverting terminal.

Op-amp input currents produce voltage drops I_{B1} x R_s and I_{B2} x R_1 across the resistors. Rs and R1 should be selected as equal resistors so that the resistor voltage drops are approximately equal. Any difference in these voltage drops will have the same effect as an input offset voltage.

Maximum Bias Resistor Values :

If very small resistance values are selected for Rs and R1 in the circuit the voltage drops across them will be small. On the other hand, if Rs and R1 are very large the voltage drops IB1 x Rs and IB2 x R1 might be several volts. For good bias stability the maximum voltage drop across these resistors should be less than the typical forward biased V_{BE} level for the op-amp input transistors.

Usually the resistor voltage drop made at least ten times smaller than V_{BE}.

$I_{B(max)} \times R_{(max)} \approx V_{BE}/10 \approx 0.07$ V

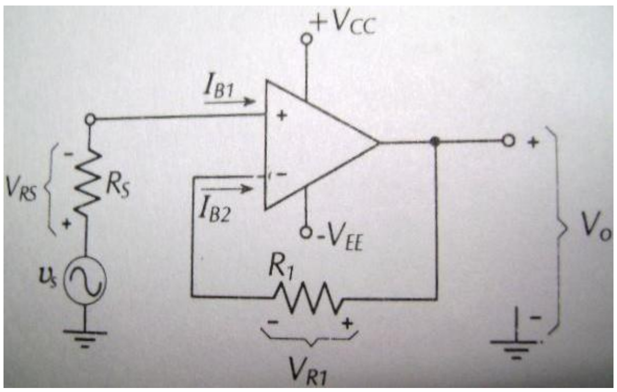
F ronthe 741 data sheet $I_{B(max)} = 500nA$.

Therefore, $R_{(max)} \approx 0.07/500nA \approx 140$ kΩ.

This is a maximum value for the bias resistors for a 741 op-amp. R(max) can be calculated using the specified I_B(max)for the particular op-amp.

$$R(max) \approx 0.1\, V_{BE}/I_B(max)$$

1.3 **Direct – Coupled Voltage Followers**

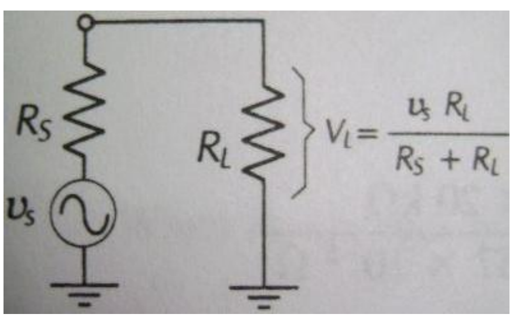


As shown in the figure the resistor R1 is frequently included in series with the inverting terminal to match the source resistance Rs in series with the non-inverting terminal.

The input and output impedances of the voltage follower are

$Z_{in} = (1+A)\, Z_i$ and $Z_{out} = Z_o \backslash (1+A)$

The voltage follower has very high input impedance and very low output impedance. Therefore, it is normally used to convert a high impedance source to low output impedance. In this situation it is said to be used as a 'buffer' between the high impedance source and the low impedance load. Thus, it is termed a 'buffer amplifier'.



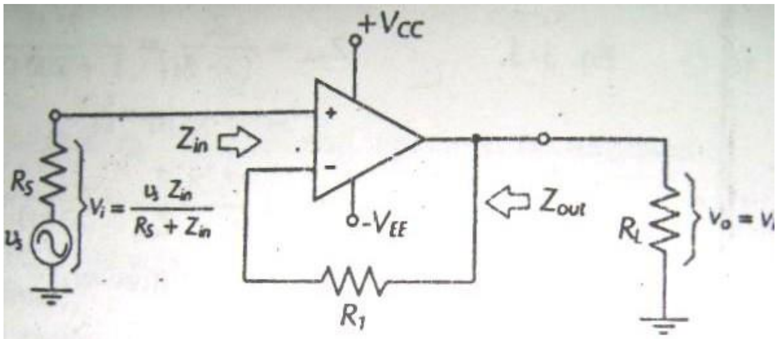
From the fig, a signal voltage is potentially divided across $R_s$and R_L when connected directly to a load. But when the load and source are joined by the voltage follower, it presents its very high impedance to the signal source. Because Z_{in} is normally very much larger than Rs, there is virtually no loss at this point and effectively all the input appears at the op-amp input.

The voltage follower output is

$V_d = \frac{V_i}{A}$ And $V_o = V_i - V_d$

$$\therefore V_o = V_i - \frac{V_i}{A}$$

$$\Rightarrow V_o = V_i\left(1 - \frac{1}{A}\right)$$



The output voltage can be thought of as being divided across RL and the voltage follower output impedance Z_{out}. But Z_{out} is much smaller than any load resistance that might be connected. So, there is effectively no signal loss and all V_i appears as V_o at the circuit output.

Example:

1. A voltage follower using a 741 op-amp is connected to a signal source via a 47kΩ. Select a suitable value for resistor R1. Also calculate the maximum voltage drop across each resistor and the maximum offset voltage produced by the input offset current.

$R_1 = R_s = 47k\Omega$

From a 741 data sheet $I_{B(max)} = 500nA$ and $I_{i(offset)} = 20nA$

$I_{B(max)1} \times R_s = I_{B(max)2} \times R_s$

$= 500nA \times 4.7k\Omega$

$= 23.5mV$

$V_{i(offset)} = I_{i(offset)} \times (R_s or R_1)$

$= 20nA \times 47k\Omega$

$= 0.94mV$

Problem 2

The voltage follower in the above problem has a 1V signal and a 20kΩ load. Calculate the load voltage

(a) When the load is directly connected to the source.
(b) When the voltage follower is between the load and the source.

Solution: (a) $V_L = \frac{V_i R_L}{R_s+R_L} = \frac{1\times 20k}{(20k+47k)} = 298mV$

(b) For 741 op-amp, $A = 2\times 10^5$, $Z_{in} = 2M\Omega$, $Z_{out} = 75\Omega$

$$Z_{inf} = (1+A)Z_{in} = (1+2\times 10^5)\times 2M$$

$$= 4\times 10^{11}\Omega$$

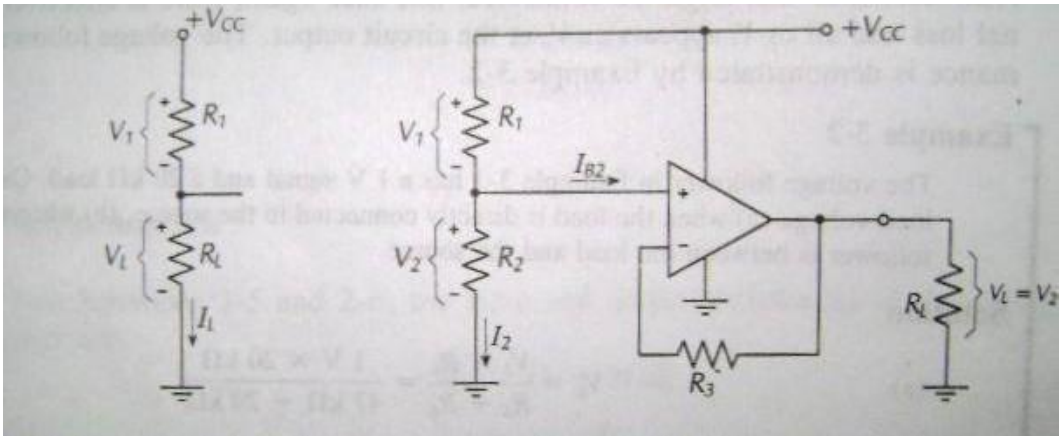
$$V_i = \frac{V_s \times Z_{inf}}{Z_{inf}+R_s} = \frac{1\times 4\times 10^{11}}{4\times 10^{11}+47k} \approx 1V effectively$$

$$V_o = V_i\left(1-\frac{1}{A}\right) = 1\left(1-\frac{1}{200000}\right) = 1V effectively$$

$$Z_{outf} = \frac{Z_o}{1+A} = \frac{75}{1+200000} = 37\times 10^{-5}\Omega$$

$$V_L = \frac{V_o \times R_L}{R_L + Z_{outf}} = \frac{1\times 20k}{20k+37\times 10^{-5}} \approx 1V$$

When the voltage follower is used with a potential divider to produce a low impedance dc voltage source, as in fig (a), load resistor R_L is directly connected in series with R_1 to derive a voltage V_L from the supply V_{CC}. This simple arrangement has the disadvantage that the V_L varies if the load resistance changes. In fig (b), the presence of the voltage follower maintains the VL constant regardless of the load resistance.



(a) V_L derived directly from V_{CC} varies when R_L varies
(b) A potential divider and voltage follower produces a constant V_L

Example:

A 1 kΩ load resistor is to have 5V developed across it from a 15V source. Design suitable circuits as shown above circuit fig (a) and (b) and calculate he load voltage variation in each case when the load resistance varies by -10%. Use a 741 op-amp.

Solution: For circuit in fig. (a)

$$I_L = \frac{V_L}{R_L} = \frac{5}{1k} = 5mA$$

$$V_1 = V_{cc} - V_L = 15 - 5 = 10V$$

$$R_i = \frac{V_1}{I_L} = \frac{10}{5m} = 2k\Omega$$

When R_L changes by -10%

$$V_L = \frac{V_{cc} \times (R_L - 10\%)}{(R_L - 10\%) + R_f} = \frac{15 \times (1k - 10\%)}{(1k - 10\%) + 2k} = 4.66V$$

For circuit in fig. (b) $V_2 = V_L = 5V and V_1 = V_{cc} - V_2 = 10V$

For 741 $I_{B(max)} = 500nA and I_2 = 100 I_{B(max)} = 50\mu A$

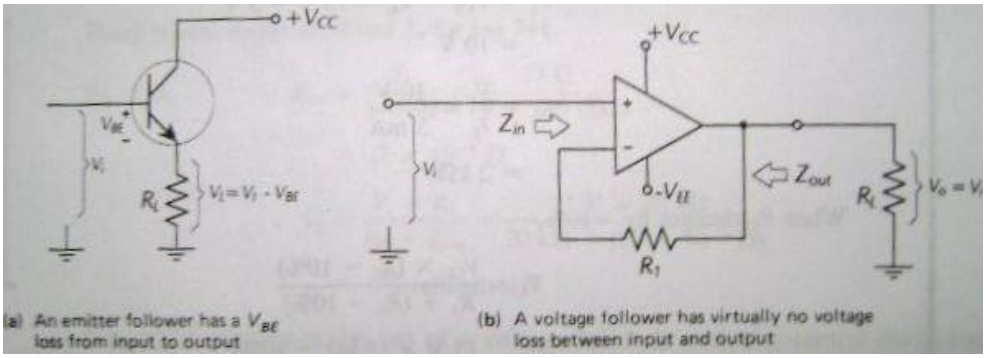
$$R_2 = \frac{V_2}{I_2} = \frac{5}{50\mu} = 100k\Omega$$

$$R_1 = \frac{V_1}{I_2} = \frac{10}{50\mu} = 200k\Omega$$

When R_L changes by -10%

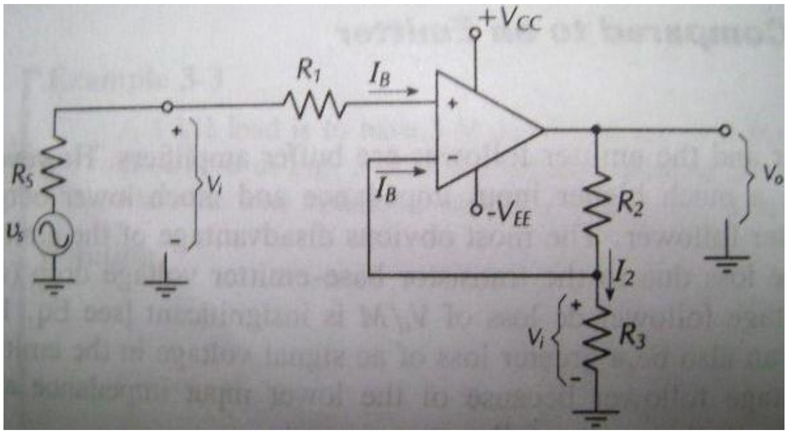
$$V_L = V_2 = 5V effectively$$

Voltage Follower compared to an Emitter Follower



- Both voltage follower and the emitter follower are buffer amplifiers.
- The voltage follower has a much higher input impedance and much lower output impedance than the emitter follower.
- The disadvantage of the emitter follower is the dc voltage loss due to the transistor base-emitter voltage drop. But the voltage follower dc loss of V_i/A is insignificant.
- There can also be a greater loss of ac signal voltage in the emitter follower than in the voltage follower because of the lower input impedance and higher output impedance with the emitter follower.

1.4 **Direct coupled non-inverting amplifiers:**



The voltage gain of a non-inverting amplifier,

$$A_f = 1 + \frac{R_f}{R_2}$$

As always with a bipolar op-amp, design commences by selecting the potential divider current (I_2) very much larger than the maximum input bias current I_B(max).

Because $V_{R2} = V_i$ (virtual short)

$R_2 = V_i/I_2$

And V_o appears across (R_2 + R_f).

So, $R_2 + R_f = V_o/I_2$

Finally, to equalize the I_BR voltage drops at the op-amp input, R1 is calculated as

$R_{com} \approx R2 \parallel R3$

If R1 is not very much larger than the source resistance,

$Rs + R_{com} \approx R2 \parallel R3$

Example

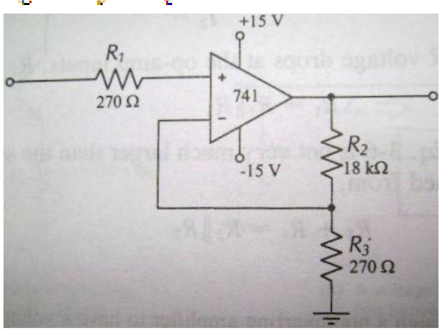
Using a 741 op-amp design a non-inverting amplifier to have a voltage gain of approximately 66. The signal amplitude is to be 15mV.

Solution :

$I_{B(max)} = 500nA \therefore I_2 = 100 \times I_{B(max)} = 50\mu A$

$$R_2 = \frac{V_i}{I_2} = \frac{15m}{50\mu} = 300\Omega$$

$V_o = A_v \times V_i = 66 \times 15m = 990mV$



$$R_2 + R_f = \frac{V_o}{I_2} = \frac{990m}{50\mu} = 19.8k\Omega$$

$$R_f = (R_2 + R_f) - R_2 = 19.5k\Omega$$

$$\therefore R_{com} = R\_2 \parallel R\_f \approx 295\Omega$$

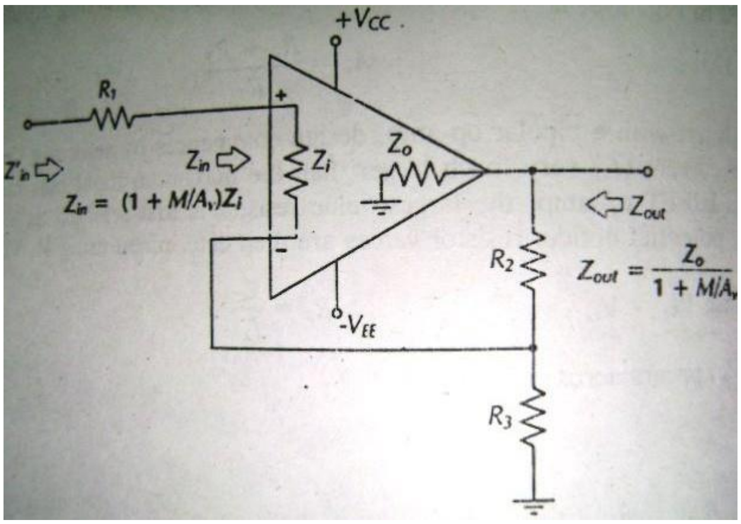
Performance

The input impedance of the op-amp circuit is,1

$$Z_{inf} = (1 + A\beta)Z_{in}$$

$$\beta = \frac{R_1}{R_1 + R_f} = \frac{1}{A_f}$$

$$\therefore Z_{inf} = \left(1 + \frac{A}{A_f}\right)Z_{in}$$



The impedance seen from the signal source is,

$$Z'_{inf} = R_{com} + Z_{inf}$$

Since Z_{inf} is always much larger than R_{com} in a non-inverting amplifier, the inclusion of R1 normally makes no significant difference.

The output impedance of the op-amp circuit is,

$$Z_{outf} = \frac{Z_{out}}{1 + A\beta}$$

$$\because \beta = \frac{1}{A_f} \therefore Z_{outf} = \frac{Z_{out}}{1 + \frac{A}{A_f}}$$

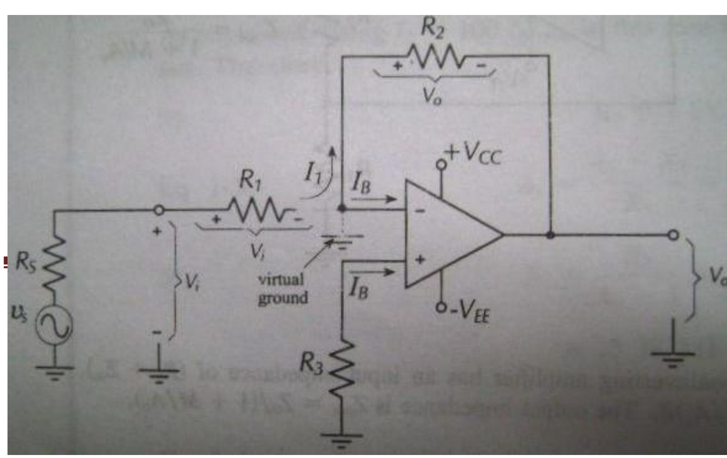
Problem

Calculate the input impedance of the non-inverting amplifier as shown below . Use the typical parameters for the LF 353 op-amp.

Solution: For LF 353 A=100000 and $Z_{in} = 10^{12}\Omega$

$$\because Z_{inf} = \left(1 + \frac{A}{A_f}\right)Z_{in} \approx 1.5 \times 10^{15}\Omega$$

$$and\, Z'_{inf} = R_{com} + Z_{inf} \approx 1.5 \times 10^{15}\Omega$$



1.5 **Direct - Coupled Inverting Amplifier:**

Resistor R_{com} is included at the non-inverting terminal to equalize the dc voltage drops due to the input bias currents approximately equal resistance should be 'seen' when 'looking out' from input terminal of the op-amp .

Therefore, $R_{com} \approx R_1 \| R_f$

And if R_f is not very much larger than the source resistance, then

$R_{com} \approx (R_1 = R_s) \| R_f$

As with other bipolar op-amp circuits, the resistor current (I_1) is first selected very much larger than the maximum input bias current ($I_{B\,max}$).

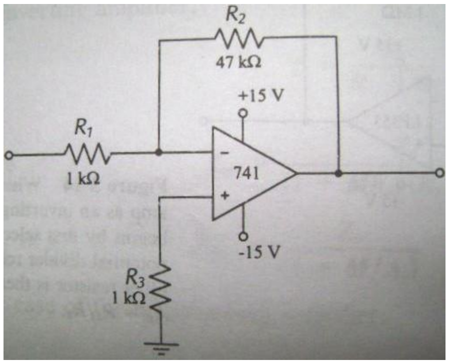
$$R_1 = \frac{V_i - V_2}{I_1} = \frac{V_i}{I_1} \; [\because V_2 = 0]$$

Since op-amp input terminal does not draw any current so, I_1 flows to feedback resistance.

$R_f = V_o/I_1$

Example

Design an inverting amp using a 741 op-amp. The voltage gain is to be 50 and the output voltage amplitude is to be 2.5 V

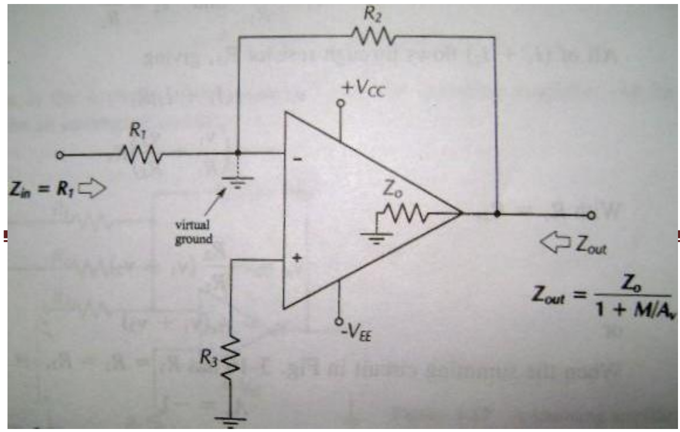


Solution:

$$I_{B(max)} = 500nA \therefore I_2 = 100 \times I_{B(max)} = 50\mu A$$

$$V_i = \frac{V_o}{A_f} = \frac{2.5}{50} = 50mV$$

$$R_1 = \frac{V_i}{I_1} = \frac{50m}{50\mu} = 1k\Omega$$



Performance

$Z_{inf} = R_1$

The output impedance of the inverting amplifier is determined exactly as for any other op-amp circuit.

$$Z_{outf} = \frac{Z_{out}}{1 + A\beta} and \beta = \frac{R_1}{R_1 + R_f}$$

$$Z_{outf} = \frac{Z_o}{\left(1 + \frac{AR_1}{R_1 + R_f}\right)}$$

$$when R_f \gg R_1 Z_{outf} = \frac{Z_{out}}{1 + \frac{A}{A_f}}$$

1.6 **Summing Amplifiers:**

Inverting Summing Circuit:

Fig below shows a circuit that amplifies the sum of two or more inputs and since inputs are applied to the inverting input terminal, hence the amplifier is called 'Inverting Summing Amplifier'.
V_a, V_b and V_c are three inputs applied to the inverting terminal through resistors R_a, R_b and R_c.
Applying Kirchoff's law at node V2

$$I_a + I_b + I_c = I_f$$

$$\Rightarrow \frac{V_a - V_2}{R_a} + \frac{V_b - V_2}{R_b} + \frac{V_c - V_2}{R_c} = \frac{V_2 - V_o}{R_f}$$

Because of Virtual Ground, $V_2=0$

$$\Rightarrow \frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = \frac{-V_c}{R_f}$$

$$\Rightarrow V_o = -R_f \left(\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c}\right)$$

$$If R_a = R_b = R_c = R then V_o = \frac{-R_f}{R}(V_a + V_b + V_c) \Rightarrow V_o = A_f(V_a + V_b + V_c)$$

$$Also if R_f = R, then V_o = (V_a + V_b + V_c)$$

$$And\,if\ \frac{R_f}{R} = \frac{1}{n}\ where\ n\ is\ the\ no.\ of\ inputs.\ Here\ n = 3$$

$$\therefore \frac{R_f}{R} = \frac{1}{3} \Rightarrow V_o = -\frac{(V_a + V_b + V_c)}{3}$$

Here the output voltage is equal to the average of all the three inputs. Hence this can be used as an 'Averaging Circuit'.

Non-Inverting Summing Circuit:

Here the three inputs are connected to the non-inverting input through resistors of equal value R. The voltage V_1 is determined using superposition theorem. Let V_b and V_c are grounded and let V_{1a} be at V_1 due to V_a, corresponding voltage.

$$V_{1a} = \frac{V_a \times R\backslash 2}{R + R\backslash 2}$$

Similarly when V_a and V_c are grounded, then

$$V_{1b} = \frac{V_b \times R\backslash 2}{R + R\backslash 2}$$

When V_a and V_b are grounded, then

$$V_{1c} = \frac{V_c \times R\backslash 2}{R + R\backslash 2}$$

$$V_1 = V_{1a} + V_{1b} + V_{1c} = \frac{V_a}{3} + \frac{V_b}{3} + \frac{V_c}{3}$$

The output voltage is $V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$

$$V_o = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{V_a + V_b + V_c}{3}\right)$$

$$If \left(1 + \frac{R_f}{R_1}\right) = 3 \quad ie.\ the\ no.\ of\ inputs$$

$$then\ V_o = V_a + V_b + V_c$$

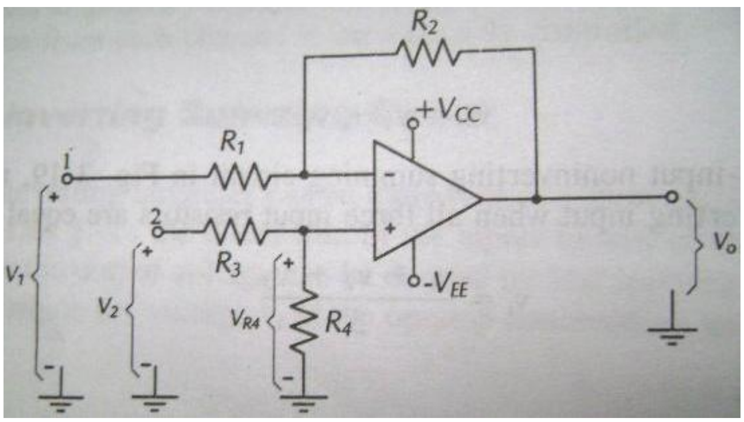
Output voltage is equal to the sum of all the three input voltages.

If the gain of the amplifier is 1 I.e. $\left(1+\frac{R_f}{R_i}\right) = 1$, then the output is,

$$V_o = \frac{(V_a + V_b + V_c)}{3}$$

1.7 Difference Amplifier:

A difference amplifier or a differential amplifier amplifies the difference between two input signals. A differential amplifier is a combination of inverting and non-inverting configurations. V_y and V_x are two inputs applied to inverting and non-inverting input terminals respectively. Apply superposition theorem to determine the output voltage Vo.



When $V_x = 0$, the configuration becomes an inverting amplifier and hence the output is

$$V_{oy} = -\frac{RF}{R1} V_y$$

When $V_y = 0$, the configuration is a non-inverting amplifier. Hence the output is,

$$V_{ox} = \left(1+\frac{R_f}{R_1}\right) V_1$$

$$V_1 = \frac{R_3}{R_2+R_3} V_x$$

$$\Rightarrow V_{ox} = \left(\frac{R_3}{R_2+R_3}\right)\left(1+\frac{R_f}{R_1}\right) V_x$$

$$Let R_{23} = R_1 and R_f = R_3, then V_{ox} = \frac{R_f}{R_1} V_x$$

$\therefore$ The total output voltage is,

$$V_o = V_{oy} + V_{ox}$$

$$= \frac{R_f}{R_1} V_x - \frac{R_f}{R_1} V_y$$

$$\Rightarrow V_o = \frac{R_f}{R_1}(V_x - V_y)$$

When RF and R1 are equal value resistors, the output is the direct difference of the two inputs. By selecting RF greater than R1 the output can be made an amplified version of the input difference.

Input Resistance

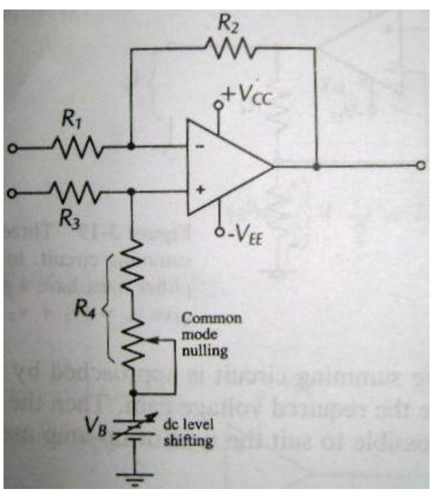
Problems with selecting the difference amplifier resistors as R1 = R2 and RF = R3 is that the two input resistances are unequal. The input resistance for voltage at inverting terminal is R1 as in the case of an inverting amplifier. At the op-amp non-inverting input terminal, the input resistance is very high, as it is for a non-inverting amplifier.

From the output voltage equation it is shown that he same result would be obtained if he ratio RF/R1 is the same as R3/R2 instead of making RF = R3 and R1 = R2.
Therefore, when the resistance of R1 has been determined, R2 = R3 can be made equal to R1, as long as the ratio of the resistance is correct. This will give equal input resistances at the two input terminals of the circuit.

There are two types of differential input resistance $(R_{i(diff)})$ and common mode input resistance (R_{icom}).

The differential input resistance is the resistance offered to a signal source which is connected directly across the input terminals. It is the sum of the two input resistances.

$R_{i(diff)} = R_1 + R_2 + R_3$



The common mode input resistance is the resistance offered to a signal source which is connected between the ground and both input terminals, that is, the parallel combination of the two input resistances.

$R_{i(cm)} = R_1 \parallel (R_2 + R_3)$

Common Mode Voltage

If the ratio R_F/R_1 and R_3/R_2 are not exactly equal, one input voltage will be amplified by a greater amount than the other. Also, the common mode voltage at one input will be amplified by a greater amount than that at the other input. Consequently, common mode voltages will not be completely cancelled. One way of minimizing the common mode input from a difference amplifier is as shown in the fig below.

R_3 is made up of a fixed value resistor and a much smaller adjustable resistor . This allows the ratio R_3/R_2 to be adjusted to closely match R_F/R_1 in order to null the common mode output voltage to zero.

Output Level Shifting

R_3 is connected to a VB instead of grounding it in the usual way. To understand the effect of V_B, assume that both input voltages are zero. The voltage at the op-amp non-inverting input terminal will be $V_f = \frac{V_B \times R_2}{R_3 + R_2}$

The voltage at the op-amp inverting input terminal will be ,

$$V_- = V_+$$

The output will be, $Vo = \left(\frac{R_1 + R_F}{R_1}\right) V_+$

Substituting for V+ and using the resistor relationships ($\frac{RF}{R1} = \frac{R3}{R2}$), the output voltage is ,

$$V_o = V_B$$

Therefore, if VB is adjustable, the dc output voltage level can be shifted as desired.

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