Chapter 2. - DC Biasing - BJTs

Objectives

To Understand :

- Concept of Operating point and stability
- Analyzing Various biasing circuits and their comparison with respect to stability

BJT – A Review

- Invented in 1948 by Bardeen, Brattain and Shockley
- Contains three adjoining, alternately doped semiconductor regions: Emitter (E), Base (B), and Collector (C)
- The middle region, base, is very thin
- Emitter is heavily doped compared to collector. So, emitter and collector are not interchangeable.

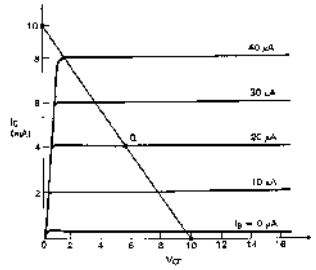
Three operating regions

- **Linear** – **region** operation:
  - Base – emitter junction forward biased
  - Base – collector junction reverse biased
- **Cutoff** – **region** operation:
  - Base – emitter junction reverse biased
  - Base – collector junction reverse biased
- **Saturation** – **region** operation:
  - Base – emitter junction forward biased
  - Base – collector junction forward biased

Three operating regions of BJT

- Cut off: $V_{CE} = V_{CC}$, $I_C \cong 0$
- Active or linear : $V_{CE} \cong V_{CC}/2$, $I_C \cong I_{C\,max}/2$
- Saturation: $V_{CE} \cong 0$, $I_C \cong I_{C\,max}$

Q-Point (Static Operation Point)



- The values of the parameters I_B, I_C and V_{CE} together are termed as 'operating point' or Q (Quiescent) point of the transistor.

Q-Point

- The intersection of the dc bias value of I_B with the dc load line determines the *Q*-point.
- It is desirable to have the *Q*-point centered on the load line. Why?
- When a circuit is designed to have a centered *Q*-point, the amplifier is said to be midpoint biased.
- Midpoint biasing allows optimum ac operation of the amplifier.

Introduction - Biasing

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system.In fact, the amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal

- The analysis or design of any electronic amplifier therefore has two components:
  - The dc portion and
  - The ac portion

During the design stage, the choice of parameters for the required dc levels will affect the ac response.

What is biasing circuit?

- Once the desired dc current and voltage levels have been identified, a network must be constructed that will establish the desired values of I_B, I_C and V_{CE}, Such a network is known as biasing circuit. A biasing network has to preferably make use of one power supply to bias both the junctions of the transistor.

Purpose of the DC biasing circuit

- To turn the device "ON"
- To place it in operation in the region of its characteristic where the device operates most linearly, i.e. to set up the initial dc values of I_B, I_C, and V_{CE}

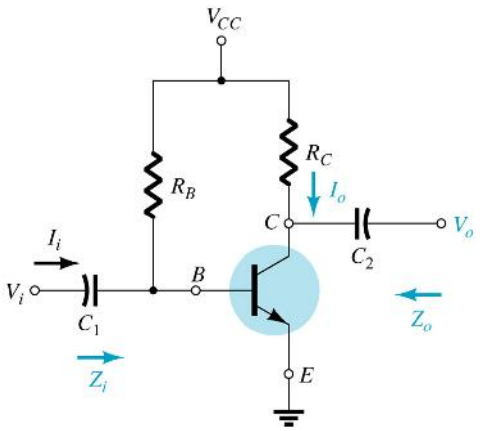
Important basic relationship

- $V_{BE} = 0.7V$
- $I_E = (\beta + 1)\, I_B \cong I_C$
- $I_C = \beta\, I_B$

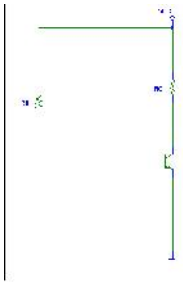
Biasing circuits:

- Fixed – bias circuit
- Emitter bias
- Voltage divider bias
- DC bias with voltage feedback
- Miscellaneous bias

Fixed bias



- The simplest transistor dc bias configuration.
- For dc analysis, open all the capacitance.



DC Analysis

- Applying KVL to the input loop:

$$V_{CC} = I_B R_B + V_{BE}$$

- From the above equation, deriving for IB, we get,

$$I_B = [V_{CC} - V_{BE}] / R_B$$

- The selection of R_B sets the level of base current for the operating point.
- Applying KVL for the output loop:

$$V_{CC} = I_C R_C + V_{CE}$$

- Thus,

$$V_{CE} = V_{CC} - I_C R_C$$

- In circuits where emitter is grounded,

$$V_{CE} = V_E$$
$$V_{BE} = V_B$$

Design and Analysis

- **Design**: Given – I_B, I_C , V_{CE} and V_{CC}, or I_C , V_{CE} and β, design the values of R_B, R_C using the equations obtained by applying KVL to input and output loops.

- **Analysis**: Given the circuit values (V_{CC}, R_B and R_C), determine the values of I_B, I_C , V_{CE} using the equations obtained by applying KVL to input and output loops.

Problem – Analysis

Given the fixed bias circuit with V_{CC} = 12V, R_B = 240 kΩ, R_C = 2.2 kΩ and β = 75. Determine the values of operating point.

Equation for the input loop is:

$$I_B = [V_{CC} – V_{BE}] / R_B \text{ where } V_{BE} = 0.7V,$$

thus substituting the other given values in the equation, we get

$$I_B = 47.08uA$$
$$I_C = \beta I_B = 3.53mA$$
$$V_{CE} = V_{CC} – I_C R_C = 4.23V$$

- When the transistor is biased such that I_B is very high so as to make I_C very high such that $I_C R_C$ drop is almost V_{CC} and V_{CE} is almost 0, the transistor is said to be in saturation.

$$I_C \text{ sat} = V_{CC} / R_C \quad \text{in a fixed bias circuit.}$$

Verification

- Whenever a fixed bias circuit is analyzed, the value of I_{CQ} obtained could be verified with the value of I_{CSat} (= V_{CC} / R_C) to understand whether the transistor is in active region.
- In active region,

$$I_{CQ} = (I_{CSat} /2)$$

Load line analysis

A fixed bias circuit with given values of V_{CC}, R_C and R_B can be analyzed (means, determining the values of I_{BQ}, I_{CQ} and V_{CEQ}) using the concept of load line also. Here the input loop KVL equation is not used for the purpose of analysis, instead, the output characteristics of the transistor used in the given circuit and output loop KVL equation are made use of.

- The method of load line analysis is as below:

1. Consider the equation $V_{CE} = V_{CC} – I_C R_C$ This relates V_{CE} and I_C for the given I_B and R_C
2. Also, we know that, V_{CE} and I_C are related through output characteristics

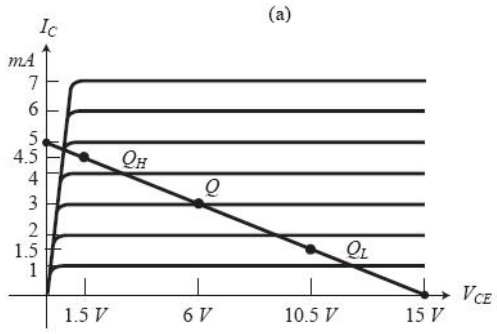
We know that the equation,

$$V_{CE} = V_{CC} – I_C R_C$$

represents a straight line which can be plotted on the output characteristics of the transistor.

Such line drawn as per the above equation is known as load line, the slope of which is decided by the value of R_C (the load).

Load line



- The two extreme points on the load line can be calculated and by joining which the load line can be drawn.
- To find extreme points, first, Ic is made 0 in the equation: $V_{CE} = V_{CC} – I_C R_C$. This gives the coordinates (V_{CC},0) on the x axis of the output characteristics.
- The other extreme point is on the y-axis and can be calculated by making $V_{CE} = 0$ in the equation $V_{CE} = V_{CC} – I_C R_C$ which gives $I_{C(\max)} = V_{CC} / R_C$ thus giving the coordinates of the point as (0, V_{CC} / R_C).
- The two extreme points so obtained are joined to form the load line.
- The load line intersects the output characteristics at various points corresponding to different I_Bs. The actual operating point is established for the given I_B.

Q point variation

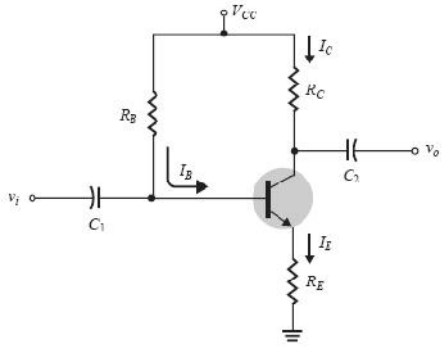
As I_B is varied, the Q point shifts accordingly on the load line either up or down depending on I_B increased or decreased respectively.

As R_C is varied, the Q point shifts to left or right along the same I_B line since the slope of the line varies. As R_C increases, slope reduces (slope is $-1/R_C$) which results in shift of Q point to the left meaning no variation in I_C and reduction in V_{CE} .

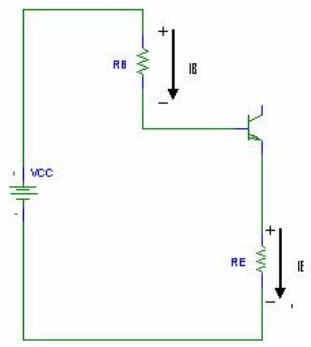
Thus if the output characteristics is known, the analysis of the given fixed bias circuit or designing a fixed bias circuit is possible using load line analysis as mentioned above.

Emitter Bias

- It can be shown that, including an emitter resistor in the fixed bias circuit improves the stability of Q point.
- Thus emitter bias is a biasing circuit very similar to fixed bias circuit with an emitter resistor added to it.



Input loop



- Writing KVL around the input loop we get,

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \quad (1)$$

We know that,

$$I_E = (\beta+1) I_B \quad (2)$$

Substituting this in (1), we get,

$$V_{CC} = I_B R_B + V_{BE} + (\beta+1) I_B R_E$$

$$V_{CC} - V_{BE} = I_B (R_B + (\beta+1) R_E)$$

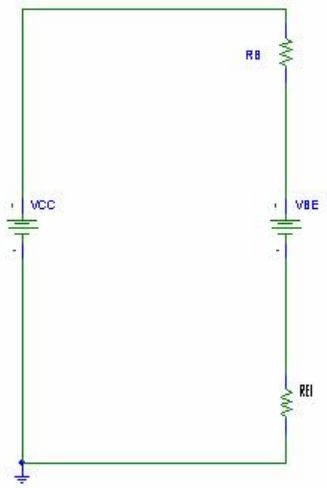
Solving for I_B:

$$I_B = (V_{CC} - V_{BE}) / [(R_B + (\beta+1) R_E)]$$

The expression for I_B in a fixed bias circuit was,

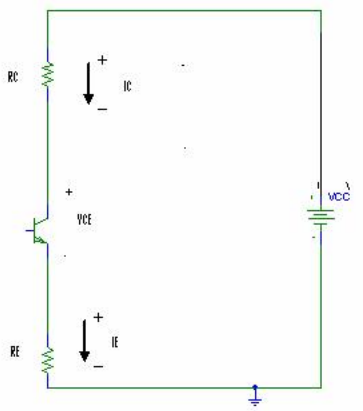
$$I_B = (V_{CC} - V_{BE}) / R_B$$

Equivalent input loop:



- R_{EI} in the above circuit is $(\beta+1)R_E$ which means that, the emitter resistance that is common to both the loops appears as such a high resistance in the input loop.
- Thus $Ri = (\beta+1)R_E$ (more about this when we take up ac analysis)

Output loop



Collector – emitter loop

Applying KVL,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

I_C is almost same as I_E

Thus,

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$= I_C (R_C + R_E) + V_{CE}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Since emitter is not connected directly to ground, it is at a potential V_E, given by,

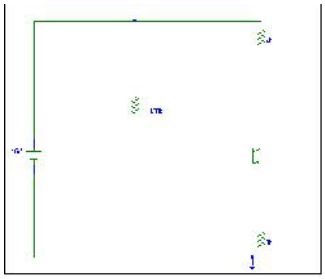
$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E \textbf{ OR } V_C = V_{CC} - I_C R_C$$

$$\text{Also, } V_B = V_{CC} - I_B R_B \textbf{ OR } V_B = V_{BE} + V_E$$

Problem:

Analyze the following circuit: given
$\beta = 75$, $V_{CC} = 16V$, $R_B = 430k\Omega$, $R_C = 2k\Omega$ and $R_E = 1k\ \Omega$



Solution:

$I_B = (V_{CC} - V_{BE}) / [(R_B + (\beta+1) R_E)]$

$= (16 - 0.7) / [430k + (76) 1k] = 30.24\mu A$

$I_C = (75) (30.24\mu A) = 2.27mA$

$V_{CE} = V_{CC} - I_C (R_C + R_E) = 9.19V$

$V_C = V_{CC} - I_C R_C = 11.46V$

$V_E = V_C - V_{CE} = 2.27V$

$V_B = V_{BE} + V_E = 2.97V$

$V_{BC} = V_B - V_C = 2.97 - 11.46 = - 8.49V$

Improved bias stability

- Addition of emitter resistance makes the dc bias currents and voltages remain closer to their set value even with variation in
  - transistor beta
  - temperature

Stability

In a fixed bias circuit, I_B does not vary with β and therefore whenever there is an increase in β, I_C increases proportionately, and thus V_{CE} reduces making the Q point to drift towards saturation.In an emitter bias circuit, As β increases, I_B reduces, maintaining almost same I_C and V_{CE} thus stabilizing the Q point against β variations.

Saturation current

In saturation V_{CE} is almost 0V, thus

$$V_{CC} = I_C (R_C + R_E)$$

Thus, saturation current

$$I_{C,sat} = V_{CC} / (R_C + R_E)$$

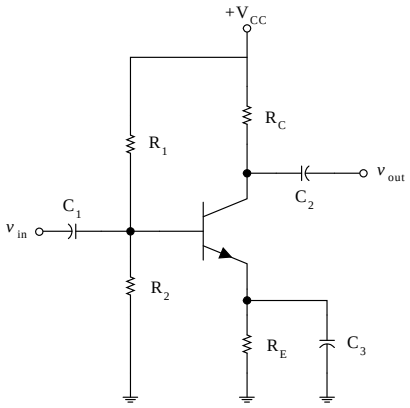
Load line analysis

The two extreme points on the load line of an emitter bias circuit are,

($0, V_{CC} / [R_C + R_E]$) on the Y axis, and

(V_{CC}, 0) on the X axis.

Voltage divider bias

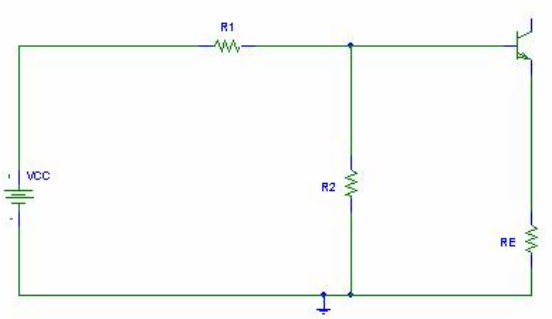


This is the biasing circuit wherein, I_{CQ} and V_{CEQ} are almost independent of β.
The level of I_{BQ} will change with β so as to maintain the values of I_{CQ} and V_{CEQ} almost same, thus maintaining the stability of Q point.

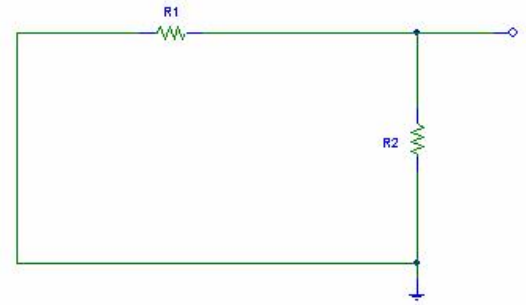
Two methods of analyzing a voltage divider bias circuit are:
Exact method – can be applied to any voltage divider circuit
Approximate method – direct method, saves time and energy, can be applied in most of the circuits.

Exact method

In this method, the Thevenin equivalent network for the network to the left of the base terminal to be found.



To find Rth:

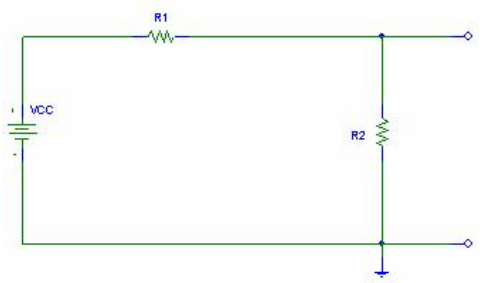


From the above circuit,

$$R_{th} = R1 \,||\, R2$$

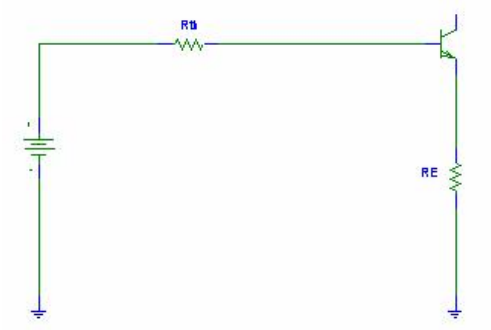
$$= R1\ R2 / (R1 + R2)$$

To find Eth



From the above circuit,

$$E_{th} = V_{R2} = R_2 V_{CC} / (R1 + R2)$$



In the above network, applying KVL

$$(E_{th} – V_{BE}) = I_B [R_{th} +(\beta + 1) R_E]$$

$$I_B = (E_{th} – V_{BE}) / [R_{th} +(\beta + 1) R_E]$$

Analysis of Output loop

KVL to the output loop:

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

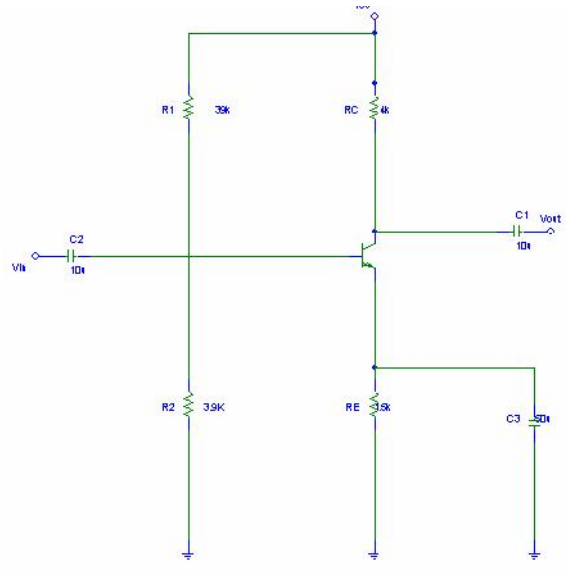
$$I_E \cong I_C$$

Thus, $$V_{CE} = V_{CC} – I_C (R_C + R_E)$$

Note that this is similar to emitter bias circuit**.**

Problem

For the circuit given below, find I_C and V_{CE}.
Given the values of R_1, R_2, R_C, R_E and $\beta = 140$ and $V_{CC} = 18V$.
For the purpose of DC analysis, all the capacitors in the amplifier circuit are opened.



Solution

Considering exact analysis:

1. Let us find $R_{th} = R1 \,||\, R2$

$= R1\,R2 / (R1 + R2) = 3.55K$

2. Then find $E_{th} = V_{R2} = R2V_{CC} / (R1 + R2)$

$= 1.64V$

3. Then find IB

$I_B = (Eth - V_{BE}) / [Rth + (\beta + 1) R_E]$

$= 4.37\mu A$

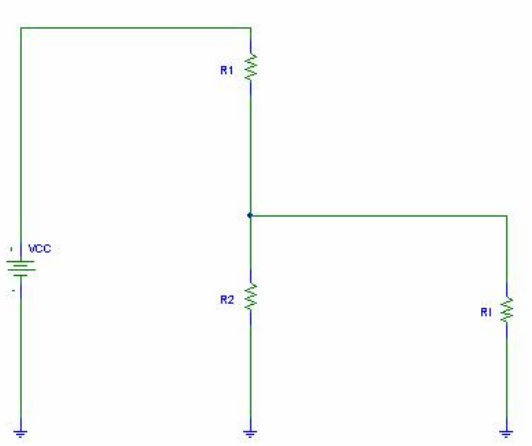
4. Then find $I_C = \beta I_B = 0.612mA$

5. Then find $V_{CE} = V_{CC} - I_C (RC + RE)$
$= 12.63V$

Approximate analysis:

The input section of the voltage divider configuration can be represented by the network shown in the next slide.

Input Network



The emitter resistance R_E is seen as $(\beta+1)R_E$ at the input loop.
If this resistance is much higher compared to R_2, then the current I_B is much smaller than I_2 through R_2.
This means, $Ri >> R2$

OR

$(\beta+1)R_E \geq 10R2$

OR

$\beta R_E \geq 10R2$

This makes I_B to be negligible.
Thus I_1 through R_1 is almost same as the current I_2 through R_2.
Thus R_1 and R_2 can be considered as in series.
Voltage divider can be applied to find the voltage across R_2 (V_B)

$$V_B = V_{CC}R_2 / (R_1 + R_2)$$

Once V_B is determined, V_E is calculated as,

$$V_E = V_B – V_{BE}$$

After finding V_E, I_E is calculated as,

$$I_E = V_E / R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} – I_C (R_C + R_E)$$

Problem

Given: V_{CC} = 18V, R_1 = 39k t , R_2 = 3.9k t , R_C = 4k t , R_E = 1.5k t and β = 140.
Analyse the circuit using approximate technique.
In order to check whether approximate technique can be used, we need to verify the condition,

$$\mathbf{R_E \geq 10R_2}$$

Here,

$$\mathbf{R_E = 210\ k\ t\ \ and\ 10R_2} = 39\ \mathbf{k}\ t$$

Thus the condition

$$\mathbf{R_E \geq 10R_2} \text{ satisfied}$$

Solution

- Thus approximate technique can be applied.

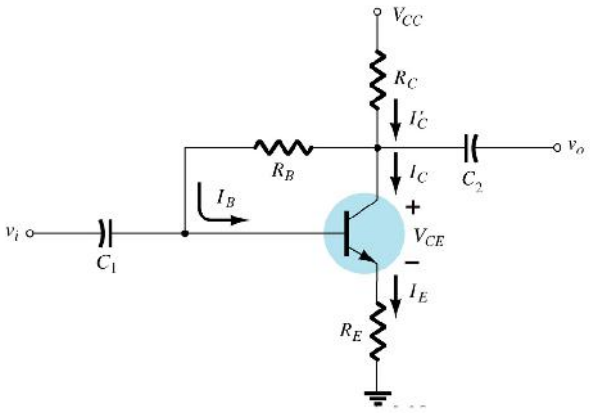
1. Find $V_B = V_{CC}R_2 / (R_1 + R_2) = 1.64V$
2. Find $V_E = V_B – 0.7 = 0.94V$
3. Find $I_E = V_E / R_E = 0.63mA = I_C$
4. Find $V_{CE} = V_{CC} – I_C(R_C + R_E) = 12.55V$

Comparison

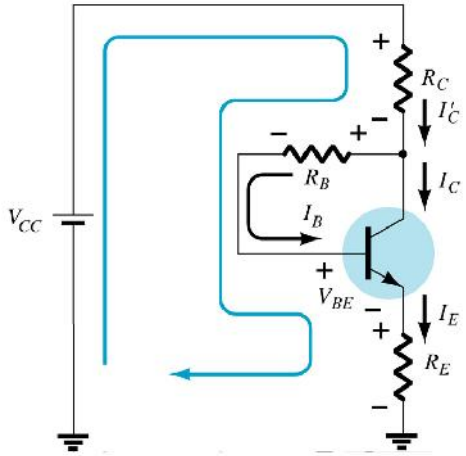
Exact Analysis	Approximate Analysis
I_C = 0.612mA	**I_C = 0.63mA**
V_{CE} = 12.63V	**V_{CE} = 12.55V**

Both the methods result in the same values for I_C and V_{CE} since the condition $\beta R_E \geq 10R_2$ is satisfied.
It can be shown that the results due to exact analysis and approximate analysis have more deviation if the above mentioned condition is not satisfied.
For load line analysis of voltage divider network, $I_{c,max} = V_{CC}/ (R_C+R_E)$ when V_{CE} = 0V and $V_{CE\ max} = V_{CC}$ when $I_C = 0$.

DC bias with voltage feedback



Input loop



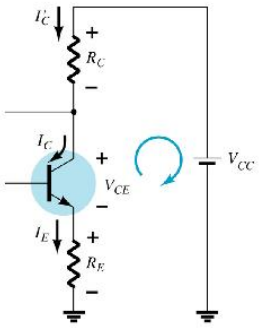
Applying KVL for Input Loop:

$V_{CC} = I_{C1}R_C + I_BR_B + V_{BE} + I_ER_E$

Substituting for I_E as $(\beta +1)I_B$ and solving for I_B,

$I_B = (V_{CC} – V_{BE}) / [R_B + \beta(R_C + R_E)]$

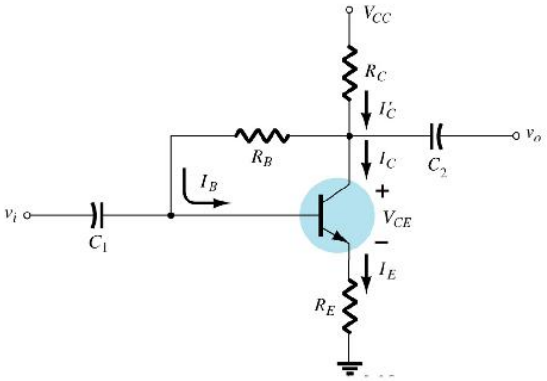
Output loop



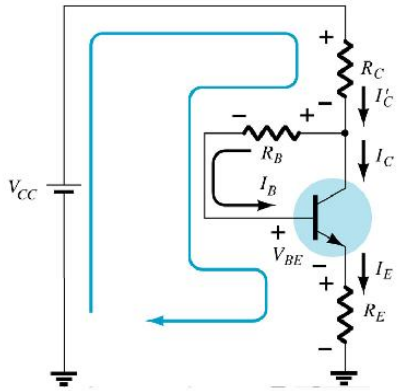
Neglecting the base current, KVL to the output loop results in,

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

DC bias with voltage feedback



Input loop



Applying KVL to input loop:

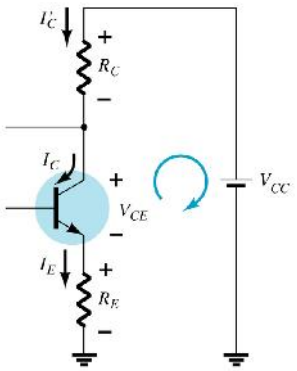
$$V_{CC} = I_C^{|}R_C + I_BR_B + V_{BE} + I_ER_E$$

$I_C^{|} \cong I_C$ and $I_C \cong I_E$

Substituting for I_E as $(\beta +1)I_B$ [or as βI_B] and solving for I_B,

$$I_B = (V_{CC} - V_{BE}) / [R_B + \beta(R_C + R_E)]$$

Output loop



Neglecting the base current, and applying KVL to the output loop results in,

$$V_{CE} = V_{CC} – I_C (R_C + R_E)$$

In this circuit, improved stability is obtained by introducing a feedback path from collector to base.
Sensitivity of Q point to changes in beta or temperature variations is normally less than that encountered for the fixed bias or emitter biased configurations.

Problem:

Given:

V_{CC} = 10V, R_C = 4.7k, R_B = 250Ω and R_E = 1.2k. β = 90.
Analyze the circuit.

$$I_B = (V_{CC} – V_{BE}) / [R_B + \beta(R_C + R_E)]$$

$$= 11.91\mu A$$

$$I_C = (\beta I_B) = 1.07mA$$

$$V_{CE} = V_{CC} – I_C (R_C + R_E) = 3.69V$$

In the above circuit, Analyze the circuit if β = 135 (50% increase).

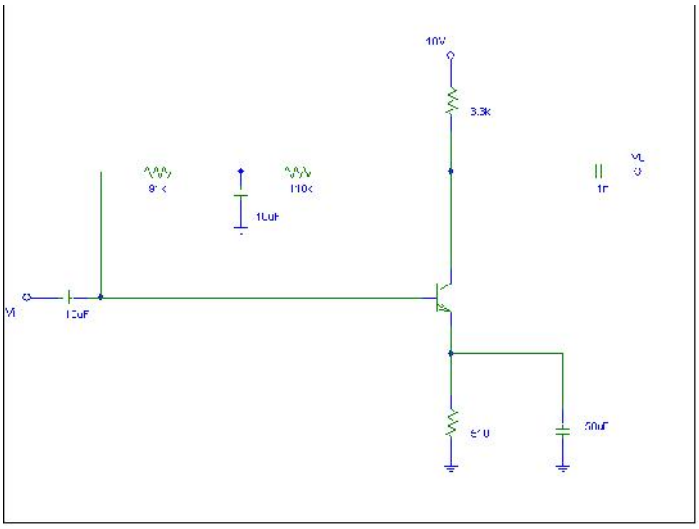
With the same procedure as followed in the previous problem, we get

- $I_B = 8.89\mu A$
- $I_C = 1.2mA$
- $V_{CE} = 2.92V$

50% increase in β resulted in 12.1% increase in I_C and 20.9% decrease in V_{CEQ}

Problem 2:

Determine the DC level of I_B and V_C for the network shown:



Solution:

Open all the capacitors for DC analysis.

$$R_B = 91\ k\Omega + 110\ k\Omega = 201k$$

$$I_B = (V_{CC} – V_{BE}) / [R_B + \beta(R_C + R_E)]$$

$$= (18 – 0.7) / [201k + 75(3.3+0.51)]$$

$$= 35.5\mu A$$

$$I_C = \beta I_B = 2.66mA$$

$$V_{CE} = V_{CC} – (I_C R_C)$$

$$= 18 – (2.66mA)(3.3k)$$

$$= 9.22V$$

Load line analysis

The two extreme points of the load line $I_{C,max}$ and $V_{CE,\ max}$ are found in the same as a voltage divider circuit.

$I_{C,max} = V_{CC} / (R_C + R_E)$ – Saturation current

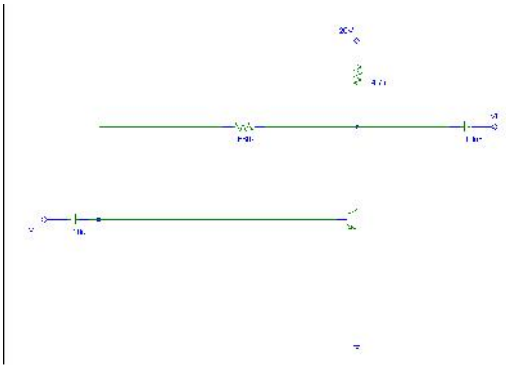
$V_{CE,\ max}$ – Cut off voltage

Miscellaneous bias configurations

There are a number of BJT bias configurations that do not match the basic types of biasing that are discussed till now.

Miscellaneous bias (1)

Analyze the circuit in the next slide. Given $\beta = 120$



Solution

This circuit is same as DC bias with voltage feedback but with no emitter resistor. Thus the expression for I_B is same except for R_E term.

$$I_B = (V_{CC} - V_{BE}) / (R_B + \beta R_C)$$

$$= (20 - 0.7) / [680k + (120)(4.7k)]$$

$$= 15.51\mu A$$

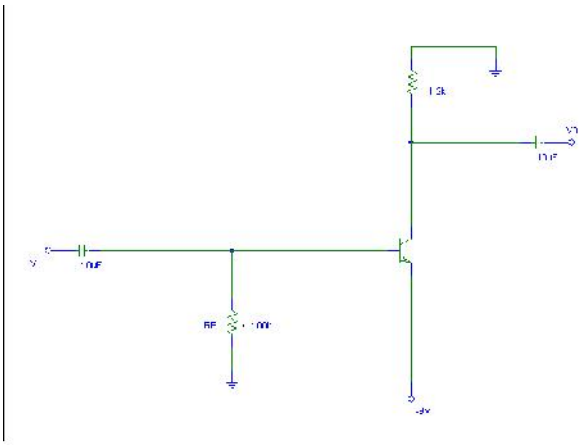
$$I_C = \beta I_B = 1.86mA$$

$$V_{CE} = V_{CC} - I_C R_C = 11.26V = V_{CE}$$

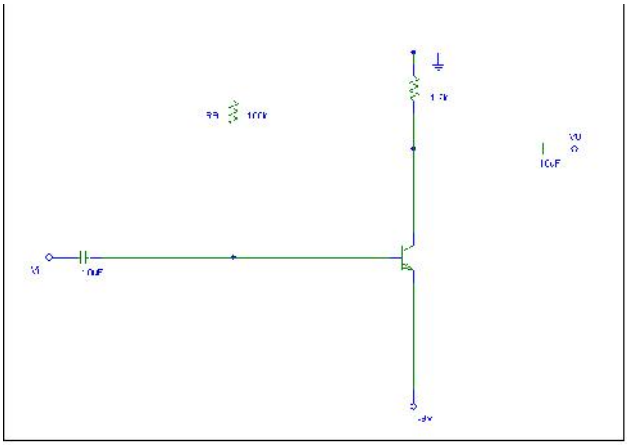
$$V_B = V_{BE} = 0.7V$$

$$V_{BC} = V_B - V_C = 0.7V - 11.26V = - 10.56V$$

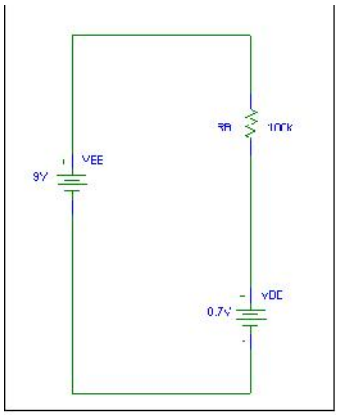
Miscellaneous bias (2)



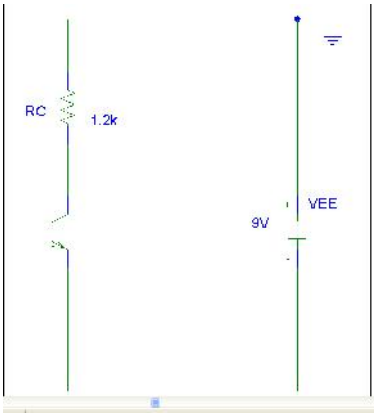
Equivalent circuit



Input loop



Output loop



Solution

The above circuit is fixed bias circuit.

Applying KVL to input loop:

$$V_{EE} = V_{BE} + I_B R_B$$

$$I_B = (V_{EE} - V_{BE}) / R_B = 83\mu A$$

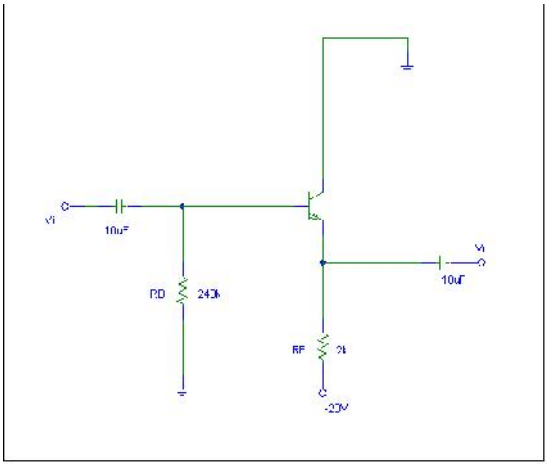
$$I_C = \beta I_B = 3.735mA$$

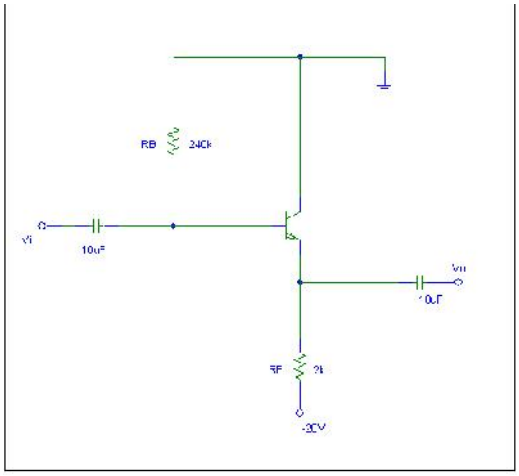
$$V_C = -I_C R_C = - 4.48V$$

$$V_B = - I_B R_B = - 8.3V$$

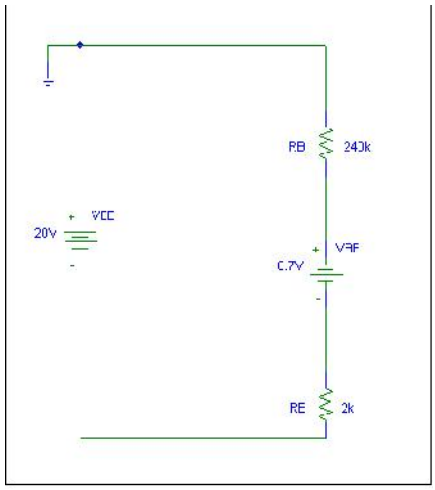
Miscellaneous bias (3)

Determine $V_{CE,Q}$ and I_E for the network.
Given $\beta = 90$
(Note that the circuit given is common collector mode which can be identified by No resistance connected to the collector output taken at the emitter)





Input loop



Writing KVL to input loop:

$$V_{EE} = I_B R_B + V_{BE} + (\beta+1) I_B R_E$$

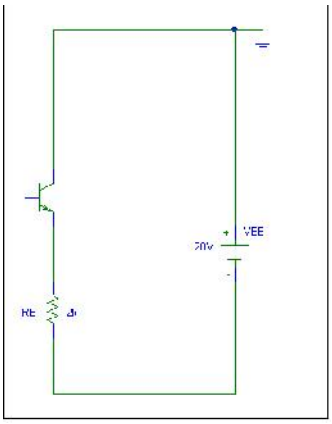
$$I_B = (V_{EE} - V_{BE}) / [R_B + (\beta+1) R_E]$$

$$= (20 - 0.7) / [240K + (91)(2K)]$$

$$= 45.73\mu A$$

$$I_C = \beta I_B = 4.12mA$$

Output loop



Applying KVL to the output loop:

$$V_{EE} = V_{CE} + I_E R_E$$

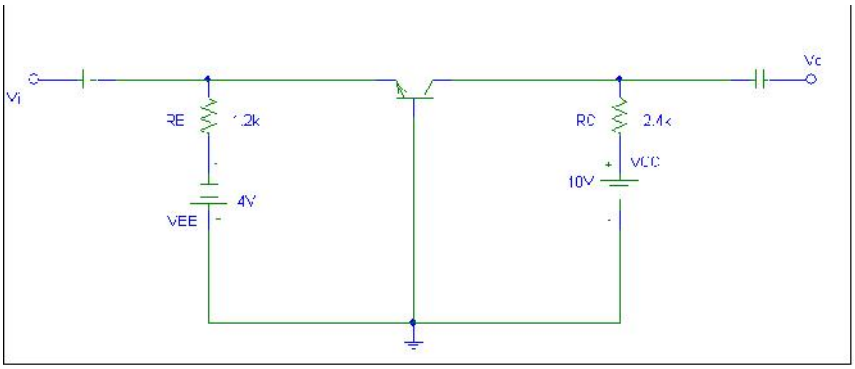
$$I_E = (\beta+1)\, I_B = 4.16\text{mA},\ V_{EE} = 20\text{V}$$

$$V_{CE} = V_{EE} - I_E R_E = 11.68\text{V}$$

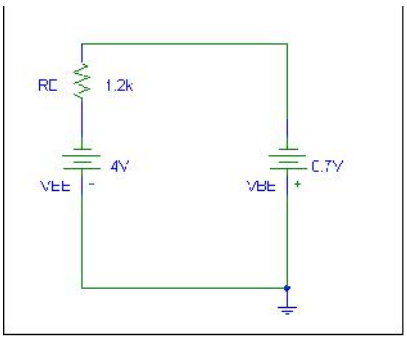
Miscellaneous bias (4)

Find V_{CB} and I_B for the Common base configuration given:

Given: $\beta = 60$



Input loop



Applying KVL to input loop

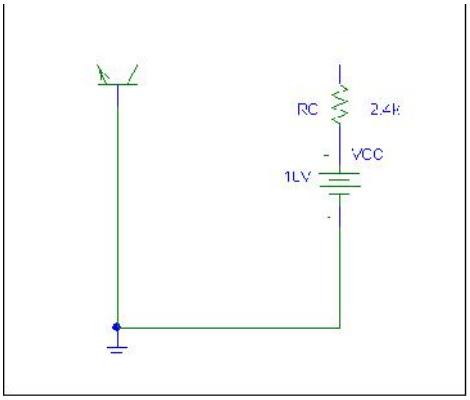
$$I_E = (V_{EE} – V_{BE}) / R_E$$

$$= 2.75mA$$

$$I_E = I_C = 2.75mA$$

$$I_B = I_C / \beta = 45.8\mu A$$

Output loop



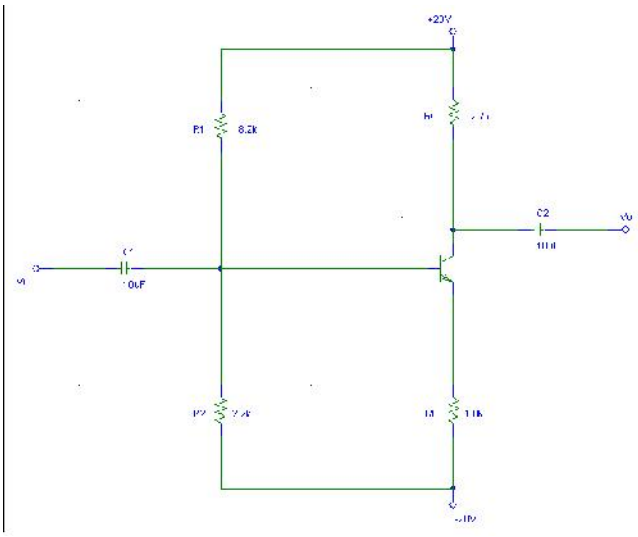
Applying KVL to output loop:

$$V_{CC} = I_C R_C + V_{CB}$$

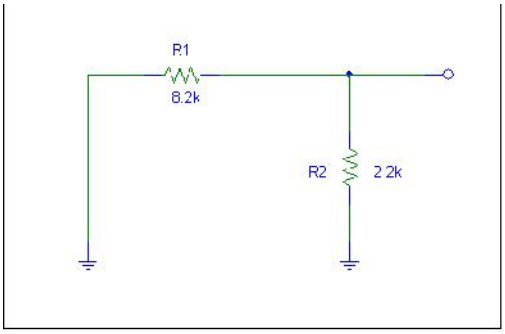
$$V_{CB} = V_{CC} – I_C R_C = 3.4V$$

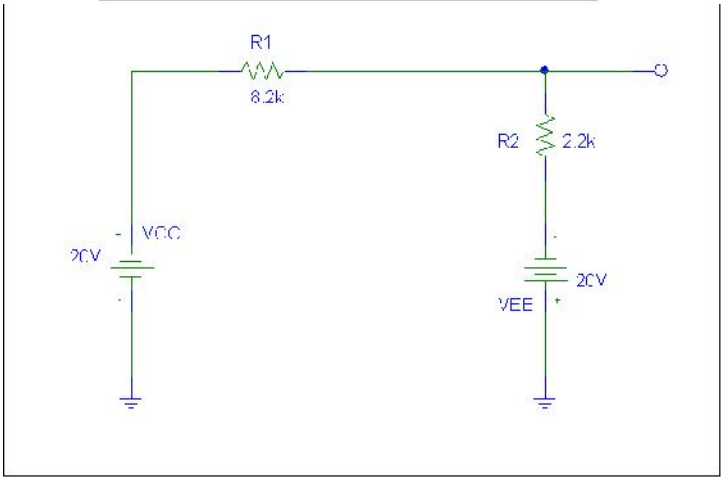
Miscellaneous bias (5)

Determine VC and VB for the network given below.
Given $\beta = 120$
Note that this is voltage divider circuit with split supply.
($+V_{CC}$ at the collector and $– V_{EE}$ at the emitter)



Thevinin equivalent at the input





R_{th}= (8.2k)(2.2k) / [8.2k+2.2k] = 1.73k

$I = (V_{CC} + V_{EE}) / [R_1 + R_2]$

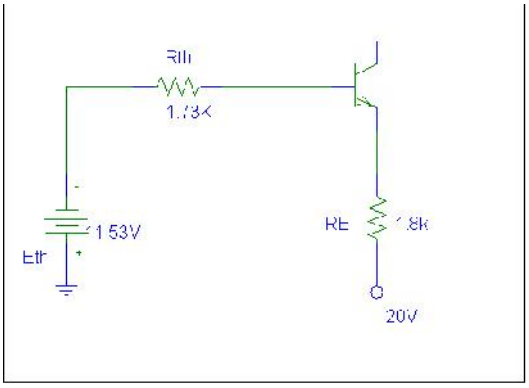
= (20 + 20) / (8.2K + 2.2K)

= 3.85mA

$E_{th} = IR_2 – V_{EE}$

= - 11.53V

Equivalent circuit



Applying KVL:

$$V_{EE} - E_{th} - V_{BE} - (\beta +1)I_BR_E - I_BR_{th} = 0$$

$$I_B = (V_{EE} - E_{th} - V_{BE}) / [(\beta +1) R_E + R_{th}]$$

$$= 35.39\mu A$$

$$I_C = \beta I_B = 4.25mA$$

$$V_C = V_{CC} - I_CR_C = 8.53V$$

$$V_B = - E_{th} - I_BR_{th} = - 11.59V$$

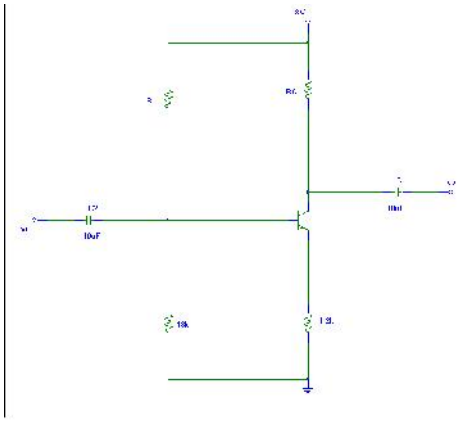
Design Operations:

Designing a circuit requires

- Understanding of the characteristics of the device
- The basic equations for the network
- Understanding of Ohms law, KCL, KVL
- If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design.
- Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen.
- Operating point needs to be recalculated with the standard values of resistors chosen and generally the deviation expected would be less than or equal to 5%.

Problem:

- Given I_{CQ} = 2mA and V_{CEQ} = 10V. Determine R_1 and R_C for the network shown:



Solution

To find R_1:

1. Find V_B. And to find V_B, find V_E because, $V_B = V_E + V_{BE}$
2. Thus, $V_E = I_E R_E$ and $I_E \cong I_C = 2mA$
   $= (2mA)(1.2k) = 2.4V$
3. $V_B = 2.4 + 0.7 = 3.1V$
4. Also, $V_B = V_{CC} R_2 / (R_1 + R_2)$
   $3.1 = (18)(18k) / R1+18k$
   Thus, $R_1 = 86.52k\Omega$

To find R_C :

Voltage across $R_C = V_{CC} – (V_{CE} + I_E R_E)$
$= 18 – [10 + (2mA)1.2k]$
$= 5.6V$
$R_C = 5.6/2mA$
$= 2.8K\Omega$

Nearest standard values are,
$R_1 = 82k\Omega + 4.7\ k\Omega = 86.7\ k\ \Omega$ where as calculated value is 86.52 k Ω .
$R_C = 2.7k$ in series with $1k = 2.8k$

both would result in a very close value to the design level.

Problem 2

The emitter bias circuit has the following specifications: $I_{CQ} = 1/2I_{sat}$, $I_{sat} = 8mA$, $V_C = 18V$, $V_{CC} = 18V$ and $\beta = 110$. Determine R_C , R_E and R_B.

Solution:

$I_{CQ} = 4mA$

$V_{RC} = (V_{CC} – V_C) = 10V$

$R_C = V_{RC} / I_{CQ}$,

$= 10/4mA = 2.5k\Omega$

To find R_E: $I_{Csat} = V_{CC} / (R_C + R_E)$

To find R_B: Find I_B where, $I_B = I_C / \beta = 36.36\mu A$

Also, for an emitter bias circuit,

$I_B = (V_{CC} – V_{BE}) / R_B+(\beta +1) R_E$

Thus, $R_B = 639.8\ k\Omega$

Standard values: $R_C = 2.4\ k\Omega$, $R_E = 1\ k\Omega$, $R_B = 620\ k\Omega$

$8mA = 28 / (2.5k + R_E)$

Thus, $R_E = 1k\Omega$

Transistor switching networks:

Through proper design transistors can be used as switches for computer and control applications.
When the input voltage V_B is high (logic 1), the transistor is in saturation (ON). And the output at its collector = V_{CE} is almost 0V(Logic 0)

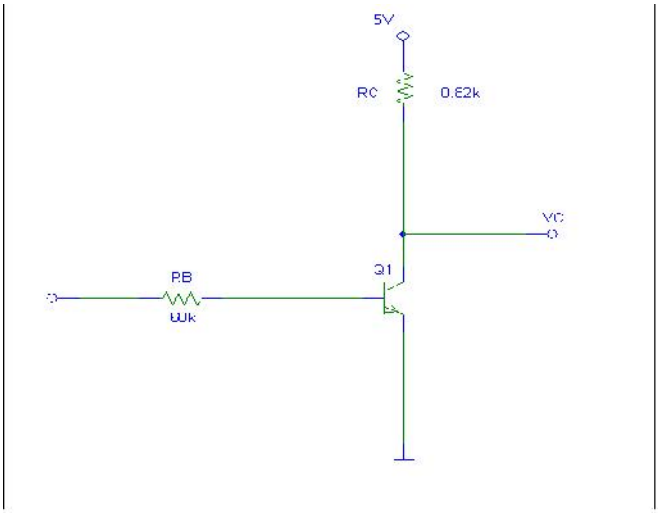
Transistor as a switch

When the base voltage V_B is low(logic 0), i.e, 0V, the transistor is cutoff(Off) and I_C is 0, drop across R_C is 0 and therefore voltage at the collector is V_{CC}.(logic 1)
Thus transistor switch operates as an inverter.
This circuit does not require any DC bias at the base of the transistor.

Design

When Vi (V_B) is 5V, transistor is in saturation and I_{Csat}
Just before saturation, $I_{B,max} = I_{C,sat} / \beta_{DC}$
Thus the base current must be greater than $I_{B,max}$ to make the transistor to work in saturation.

Analysis



When Vi = 5V, the resulting level of I_B is

$I_B = (Vi - 0.7) / R_B$

$= (5 – 0.7) / 68k$

$= 63\mu A$

$I_{Csat} = V_{CC} / R_C = 5/0.82k$

$= 6.1mA$

Verification

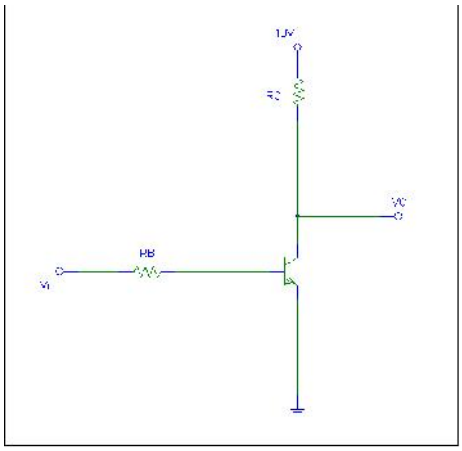
$(I_{C,sat} / \beta) = 48.8\mu A$

Thus $I_B > (I_{C,sat} / \beta)$ which is required for a transistor to be in saturation.

A transistor can be replaced by a low resistance Rsat when in saturation (switch on)
$R_{sat} = V_{CE\ sat} / I_{Csat}$ ($V_{CE\ sat}$ is very small and I_{Csat} is $I_{C,max}$ is maximum current)
A transistor can be replaced by a high resistance Rcutoff when in cutoff (switch on)

Problem

Determine R_B and R_C for the inverter of figure:



$I_{C\ sat} = V_{CC} / R_C$

$10mA = 10V / R_C$

$R_C = 1k\Omega$

I_B just at saturation $= I_{C\ sat} / \beta$

$= 10mA / 250$

$= 40\mu A$

Choose $I_B > I_{C\ sat} / \beta$, 60 μA

$I_B = (Vi – 0.7) / R_B$

60 $\mu A = (10 – 0.7) / R_B$

$R_B = 155k\Omega$

Choose $R_B = 150k\Omega$, standard value,

re calculate I_B, we get $I_B = 62\ \mu A$ which is also > $I_{C\ sat} / \beta$

Thus, $R_C = 1k$ and $R_B = 155k$

Switching Transistors

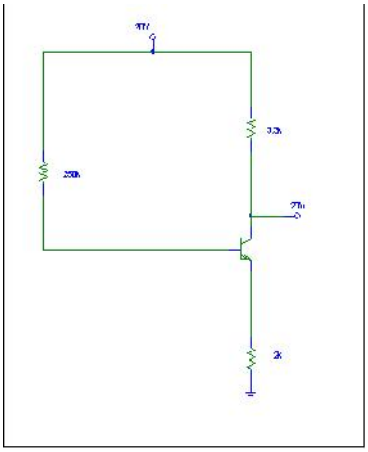
Transistor 'ON' time = delay time + Rise time
Delay time is the time between the changing state of the input and the beginning of a response at the output.
Rise time is the time from 10% to 90% of the final value.
Transistor 'OFF' time = Storage time + Fall time
For an 'ON' transistor, V_{BE} should be around 0.7V
For the transistor to be in active region, V_{CE} is usually about 25% to 75% of V_{CC}.
If V_{CE} = almost V_{CC}, probable faults:

- the device is damaged
- connection in the collector – emitter or base – emitter circuit loop is open.

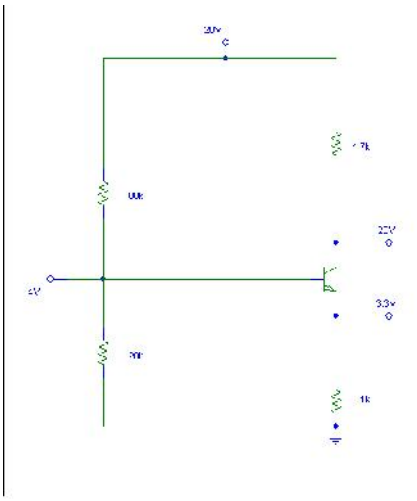
One of the most common mistake in the lab is usage of wrong resistor value.
Check various voltages with respect to ground.
Calculate the current values using voltage readings rather than measuring current by breaking the circuit.

Problem – 1

Check the fault in the circuit given.



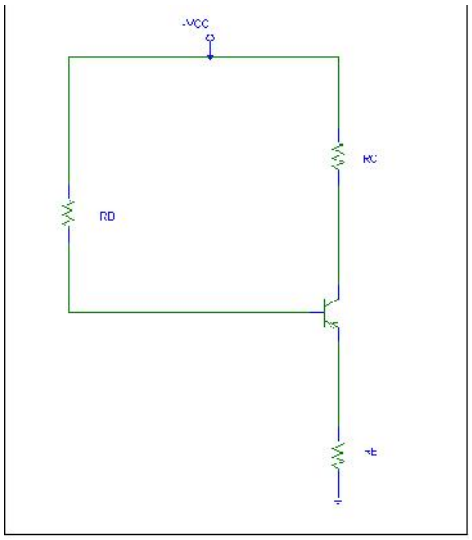
Problem - 2



PNP transistors

The analysis of PNP transistors follows the same pattern established for NPN transistors. The only difference between the resulting equations for a network in which an npn transistor has been replaced by a pnp transistor is the sign associated with particular quantities.

PNP transistor in an emitter bias



Applying KVL to Input loop:

$V_{CC} = I_B R_B + V_{BE} + I_E R_E$

Thus, $I_B = (V_{CC} - V_{BE}) / [R_B + (\beta+1) R_E]$

Applying KVL Output loop:

$V_{CE} = - (V_{CC} - I_C R_C)$

Bias stabilization

The stability of a system is a measure of the sensitivity of a network to variations in its parameters.
In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters.
β increases with increase in temperature.
Magnitude of V_{BE} decreases about 2.5mV per degree Celsius increase in temperature.
I_{CO} doubles in value for every 10 degree Celsius increase in temperature.

T (degree Celsius)	Ico (nA)	β	V_{BE} (V)
- 65	0.2 x 10-3	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3 x 103	120	0.3

Stability factors

$S (I_{CO}) = \Delta I_C / \Delta I_{C0}$

$S (V_{BE}) = \Delta I_C / \Delta V_{BE}$

$S (\beta) = \Delta I_C / \Delta \beta$

Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.
The higher the stability factor, the more sensitive is the network to variations in that parameter.

S(I_{CO})

- Analyze S(I_{CO}) for
  - emitter bias configuration
  - fixed bias configuration
  - Voltage divider configuration

For the emitter bias configuration,

$S(I_{CO}) = (\beta + 1)[1 + R_B / R_E] / [(\beta + 1) + R_B / R_E]$

If $R_B / R_E >> (\beta + 1)$, then

$S(I_{CO}) = (\beta + 1)$

For $R_B / R_E << 1$, $S(I_{CO})$ 1

Thus, emitter bias configuration is quite stable when the ratio R_B / R_E is as small as possible.
Emitter bias configuration is least stable when R_B / R_E approaches $(\beta + 1)$.

Fixed bias configuration

$S(I_{CO}) = (\beta + 1)[1 + R_B / R_E] / [(\beta + 1) + R_B / R_E]$

$= (\beta + 1)[R_E + R_B] / [(\beta + 1) R_E + R_B]$

By plugging $R_E = 0$, we get

$S(I_{CO}) = \beta + 1$

This indicates poor stability.

Voltage divider configuration

$S(I_{CO}) = (\beta + 1)[1 + R_B / R_E] / [(\beta + 1) + R_B / R_E]$

Here, replace R_B with R_{th}

$S(I_{CO}) = (\beta + 1)[1 + R_{th} / R_E] / [(\beta + 1) + R_{th} / R_E]$

Thus, voltage divider bias configuration is quite stable when the ratio R_{th} / R_E is as small as possible.

Physical impact

In a **fixed bias circuit**, I_C increases due to increase in I_{C0}. [$I_C = \beta I_B + (\beta+1) I_{C0}$]
I_B is fixed by V_{CC} and R_B. Thus level of I_C would continue to rise with temperature – a very unstable situation.

In **emitter bias circuit**, **as I_C increases**, I_E increases, V_E increases. Increase in V_E reduces I_B. $I_B = [V_{CC} – V_{BE} – V_E] / R_B$. A drop in I_B **reduces I_C**.Thus, this configuration is such that there is a reaction to an increase in I_C that will tend to oppose the change in bias conditions.

In the **DC bias with voltage feedback**, as I_C increases, voltage across R_C increases, thus reducing I_B and causing I_C to reduce.

The most stable configuration is **the voltage – divider network**. If the condition $\beta R_E >> 10R_2$, the voltage V_B will remain fairly constant for changing levels of I_C. $V_{BE} = V_B – V_E$, as I_C increases, V_E increases, since V_B is constant, V_{BE} drops making I_B to fall, which will try to offset the increases level of I_C.

$S(V_{BE})$

$S(V_{BE}) = \Delta I_C / \Delta V_{BE}$

For an emitter bias circuit, $S(V_{BE}) = - \beta / [R_B + (\beta + 1)R_E]$

If $R_E = 0$ in the above equation, we get $S(V_{BE})$ for a fixed bias circuit as,
$S(V_{BE}) = - \beta / R_B$.

For an emitter bias,

$S(V_{BE}) = - \beta / [R_B + (\beta + 1)R_E]$ can be rewritten as,

$S(V_{BE}) = - (\beta/R_E)/ [R_B/R_E + (\beta + 1)]$

If $(\beta + 1) >> R_B/R_E$, then

$$S(V_{BE}) = - (\beta/R_E)/ (\beta + 1)$$
$$= - 1/ R_E$$

The larger the R_E, lower the $S(V_{BE})$ and more stable is the system.

Total effect of all the three parameters on I_C can be written as,

$$\mathbf{aI_C = S(I_{CO})\ aI_{CO} + S(V_{BE})\ aV_{BE} + S(\ )a}$$

General conclusion:

The ratio R_B / R_E or R_{th} / R_E should be as small as possible considering all aspects of design.